

Grand Quiz Spring 2021

Subject Code CS501 lecture 1 to 22

Solved by Riz Mughal







https://www.youtube.com/channel/UCINsFwDiB62SValCcPDZbRQ/playlists

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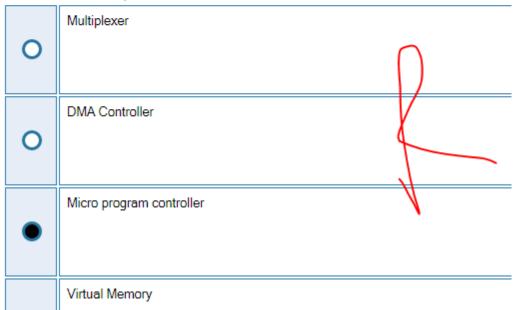




CS501:Grand Quiz

Question # 2 of 30 (Start time: 09:00:59 AM, 23 June 2021)

____ controls the sequence of the flow of microinstructions.



CS501:Grand Quiz Quiz 9 Question # 3 of 30 (Start time: 09:01:13 AM, 23 June 2021) All of the below given processors employ Little-Endian storage format except _ Select the correct option Falcon-E 0 Falcon-A **EAGLE** 0 Modified EAGLE

CS501:Grand Quiz Quiz Start Time: 09:

Question # 4 of 30 (Start time: 09:01:27 AM, 23 June 2021)

The RTL description "IO[32] \leftarrow R[5]" represents which of the following instructions of EAGLE?

0	in 32, r5
0	ori 32, r5
0	mov 32, r5
•	out 32, r5

CS501:Grand Quiz Quiz : Question # 5 of 30 (Start time: 09:01:43 AM, 23 June 2021) Which of the following is NOT related to the architecture of a computer? Select the correct option Memory addressing modes 0 Instruction set 0 Control signals I/O mechanisms

CS501:Grand Quiz Question # 6 of 30 (Start time: 09:02:03 AM, 23 June 2021) A collection of -----is called a micro program. Select the correct option large scale operations 0 DMA 0 Registers 0 Microinstructions

CS501:Grand Quiz Quiz Start T Question # 7 of 30 (Start time: 09:02:18 AM, 23 June 2021) In Type C instruction of SRC, _____ bits are allocated for constant value. Select the correct option 22 0 21 0 16 0 17 RIZ MUGHAL (SQA ENGINEER)

CS501:Grand Quiz **Quiz Start Time** Question # 8 of 30 (Start time: 09:02:33 AM, 23 June 2021) The SRC uses a hazard detection unit. The hazard can be resolved using either pipeline stalls or by _____ Select the correct option Instruction forwarding 0 Data compressing 0 Instruction handling 0 Data forwarding

CS501:Grand Quiz

Question # 9 of 30 (Start time: 09:02:48 AM, 23 June 2021)

There are _____ types of reset operations in SRC.



CS501:Grand Quiz **Quiz Start Time:** Question # 10 of 30 (Start time: 09:03:04 AM, 23 June 2021) instruction format of EAGLE processor, there is no field reserved for operands. Select the correct option Type Z Type X 0 Type Y 0 Type V RIZ MUGHAL (SQA ENGINEER)

CS501:Grand Quiz Quiz St Question # 11 of 30 (Start time: 09:03:19 AM, 23 June 2021) provides a temporary storage for the address of memory location to be accessed. Select the correct option MAR MBR 0 PC 0 LPC 0

CS501:Grand Quiz Quiz Question # 12 of 30 (Start time: 09:03:35 AM, 23 June 2021) Which one of the following registers holds the address of the next instruction to be executed? Select the correct option Instruction Register 0 Program Counter Accumulator 0 Address Mask RIZ MUGHAL (SQA ENGINEER)

CS501:Grand Quiz Quiz Start Time: 09:00 AM, 23 Ju

Question # 13 of 30 (Start time: 09:03:49 AM, 23 June 2021) Total The control signal LIR allows the IR (Instruction Register) to read the instruction which is initially stored in ______ register. Select the correct option Register A 0 MAR 0 PC 0 MBR

CS501:Grand Quiz Quiz Start

Question # 14 of 30 (Start time: 09:04:04 AM, 23 June 2021)

Execution time of a program with respect to the processor is calculated as:

Select the correct option

0

0

0

Execution Time = IC x CPI x T

Execution Time = IC x T

Execution Time = IC x CPI x MIPS

Execution Time = CPI x T x MFLOPS

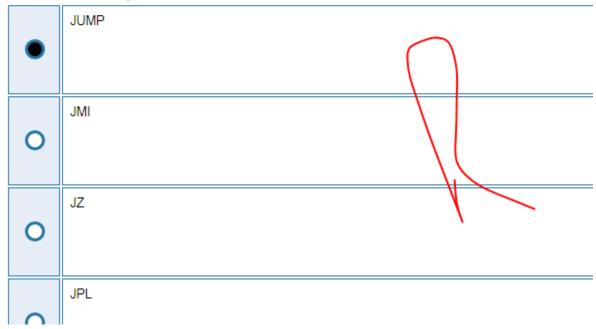
CS501:Grand Quiz Quiz S Question # 15 of 30 (Start time: 09:04:18 AM, 23 June 2021) Which of the following is NOT an advantage of register-to-register data transfer? Select the correct option Constant CPI 0 Simpler 0 Faster 0 Compact

CS501:Grand Quiz Qι Question # 16 of 30 (Start time: 09:04:32 AM, 23 June 2021) jump [ra+c2] is an _____ instruction Select the correct option Conditional jump 0 Shift 0 Unconditional jump Arithmetic and logic

CS501:Grand Quiz Quiz Start

Question # 17 of 30 (Start time: 09:04:53 AM, 23 June 2021)

Which of the following branch instructions has a condition which is always executed?



CS501:Grand Quiz Quiz Start Time: (Question # 18 of 30 (Start time: 09:05:09 AM, 23 June 2021) RTL statements separated by _____ are always executed in same clock pulse. Select the correct option Hash (#) 0 Colon (:) 0 Comma (,)

Semi-colon (;)

Question # 19 of 30 (Start time: 09:05:26 AM, 23 June 2021)

Total Mar

For any of the instructions that are a part of the instruction set of the SRC, there are certain ______ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.

	Memory
0	
0	Registers
0	None of the given
•	Control signals

Question # 20 of 30 (Start time: 09:05:41 AM, 23 June 2021)

Total Mark

Which of the following register(s) is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

0	Memory address register
0	Memory Buffer Register
•	Registers A and C
	Instruction Register

CS501:Grand Quiz Quiz Start Question # 21 of 30 (Start time: 09:05:55 AM, 23 June 2021) Which of the following is responsible for generating signals for external events? Select the correct option "CON" control signal O Interrupt generator Control unit signals generator O Exception generator

CS501:Grand Quiz Quiz Start Question # 22 of 30 (Start time: 09:06:10 AM, 23 June 2021) ____, only one field is required which specifies the type of operation. Select the correct option 3-Address Instruction 0 1-Address Instruction 0 2-Address Instruction 0 0-Address Instruction

CS501:Grand Quiz Qui Question # 23 of 30 (Start time: 09:06:25 AM, 23 June 2021) Which of the following is not a part of processor state? Select the correct option PC 0 ΙR 0 Registers 0 Stack RIZ MUGHAL (SQA ENGINEER)

CS501:Grand Quiz Quiz S Question # 24 of 30 (Start time: 09:06:41 AM, 23 June 2021) In "Jump [8]" instruction, the size of the constant field is ______ bits. Select the correct option 0 16

CS501:Grand Quiz Quiz Start

Question # 25 of 30 (Start time: 09:06:59 AM, 23 June 2021)

Which of the followings is a behavioral RTL description to enable the exceptions?

•	IE ← 1
0	IE ← -1
0	IE ← 8
0	IE ← 0

Question # 26 of 30 (Start time: 09:07:15 AM, 23 June 2021)

Total

In EAGLE processor, which of the following notations is used to represent a memory word stored at address 8?

Select the correct option

M [8]<0...15> := M [9] © M [8]

M [8]<0...15> := M [8] © M [9]

M [8]<15...0> := M [8] © M [9]

M [8]<15...0> := M [9] © M [8]

0

0

CS501:Grand Quiz

Question # 27 of 30 (Start time: 09:07:29 AM, 23 June 2021)

Which one of the following circuit design levels is called the gate level?

Select the correct option

Circuit Level

0

Machine Level

Mask Level

0

Logic Design Level

Question # 28 of 30 (Start time: 09:07:46 AM, 23 June 2021) Total The Memory Buffer Register (MBR) has a _____ connection with both the memory sub-system and the registers/ALSU. Select the correct option uni-directional 0 bi-directional tri-directional 0 zero-directional

CS501:Grand Quiz Quiz Start Question # 29 of 30 (Start time: 09:08:01 AM, 23 June 2021) The result is stored in the destination register in ______ stage of the Pipeline. Select the correct option ALU5 operation 0 Register write Instruction fetch 0 Memory access

CS501:Grand Quiz Quiz Start Tir Question # 30 of 30 (Start time: 09:08:15 AM, 23 June 2021) is an example of Miscellaneous instruction. Select the correct option Halt Call 0 Store 0 Shiftl RIZ MUGHAL (SQA ENGINEER)