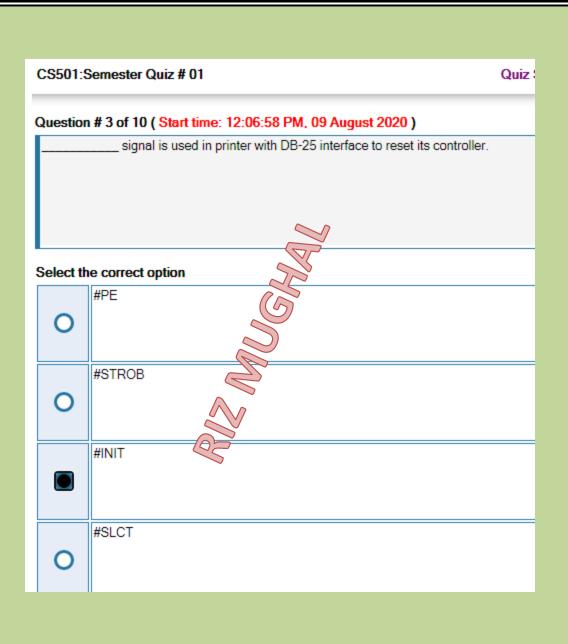
## **Cs501 Quiz(100% CORRECT)**

Solved by Rizwan Qadeer (Riz Mughal)
Youtube link:

 $\underline{https://www.youtube.com/channel/UCINsFwDiB62SValCcPDZbRQ/playlists}$ 

| CS501:5   | CS501:Semester Quiz # 01 Quiz Start Time: 12:06 PM, 09 August 2020               |                                 |  |  |  |  |
|-----------|--|---------------------------------|--|--|--|--|
| Question  | Question # 1 of 10 ( Start time: 12:06:10 PM, 09 August 2020 )  Total Marks:     |                                 |  |  |  |  |
| The info  | rmation about interrupt vector is given in 8-bits, from bit 0 to 7, which is tra | nslated to bit on the data bus. |  |  |  |  |
| Select th | ne correct option  |                                 |  |  |  |  |
|           | 16 to 23   | //                              |  |  |  |  |
| 0         | 11 to 18   | //                              |  |  |  |  |
| 0         | 0 to 7   | //                              |  |  |  |  |
| 0         | 8 to 15  | <i>1</i> ,                      |  |  |  |  |

| ect the correct option  Biased Representation  Diminished Radix Compliment Form  Sign Magnitude Form | Diminished Radix Compliment Form  Sign Magnitude Form  None of the given                        | Diminished Radix Compliment Form  Sign Magnitude Form  None of the given | stion # 2 of 10 ( Start time: 12:06:41 PM, 09 August 2020 ) is the simplest form for representing a signed number |   |
|--|---|--|---|---|
| Diminished Radix Compliment Form  Sign Magnitude Form  None of the given                             | Biased Representation  Diminished Radix Compliment Form  Sign Magnitude Form  None of the given | Diminished Radix Compliment Form Sign Magnitude Form None of the given   |   |   |
| O Diminished Radix Compliment Form Sign Magnitude Form None of the given                             | O Diminished Radix Compliment Form Sign Magnitude Form None of the given                        | Diminished Radix Compliment Form  Sign Magnitude Form  None of the given | ct the correct option   |   |
| Sign Magnitude Form  None of the given   | Sign Magnitude Form  None of the given  | Sign Magnitude Form  None of the given                                   |   |   |
| None of the given  | None of the given   | None of the given  |   | = |
|  |   |  |   |   |
|  |   |  |   |   |



| CS501:   | Semester Quiz # 01   | Quiz Start Time: 12:06 PM, 09 Au    |
|----------|--|-------------------------------------|
|          | on # 4 of 10 ( Start time: 12:07:16 PM, 09 August 2020 )         | Tota                                |
| A comp   | oonent connected to the system bus and having control of it duri | ng a particular bus cycle is called |
| Select 1 | the correct option   |                                     |
| 0        | Slave component  |                                     |
|          | Master component   |                                     |
| 0        | System bus   |                                     |
| 0        | Buffer component   |                                     |
|          |  |                                     |
|          |  |                                     |
|          |  |                                     |
|          |  |                                     |
|          |  |                                     |

| Most parallel I/O ports used with peripheral devices are mapped on a range of | O Direct memory Access  contiguous addresses | S501:    | Semester Quiz # 01 Quiz Start Time:                                    |
|---|--|----------|--|
| Direct memory Access  contiguous addresses                                    | Direct memory Access  contiguous addresses   |          |  |
| O Direct memory Access  contiguous addresses                                  | O Direct memory Access  contiguous addresses | /lost pa | rallel I/O ports used with peripheral devices are mapped on a range of |
| O Direct memory Access  contiguous addresses                                  | O Direct memory Access  contiguous addresses |          |  |
| O Direct memory Access  contiguous addresses                                  | O Direct memory Access  contiguous addresses |          |  |
| O Direct memory Access  contiguous addresses                                  | O Direct memory Access  contiguous addresses | elect th | ne correct ontion  |
| O Direct memory Access  contiguous addresses                                  | O Direct memory Access  contiguous addresses | GIGGE L  |  |
| Contiguous addresses  | Contiguous addresses                         | 0        | S  |
| Contiguous addresses  | Contiguous addresses                         |          |  |
| contiguous addresses  | contiguous addresses                         | 0        | Direct memory Access   |
|   |  |          |  |
|   |  |          | contiguous addresses   |
| Cache O   | Cache O                                      |          |  |
|   |  |          | Cache  |
|   |  | 0        |  |
|   |  |          |  |
|   |  |          |  |
|   |  |          |  |
|   |  |          |  |
|   |  |          |  |
|   |  |          |  |
|   |  |          |  |
|   |  |          |  |
|   |  |          |  |
|   |  |          |  |

| 00501.6                  | D   |  |
|--------------------------|---|--|
| CS501:Semester Quiz # 01 |   |  |
| Question                 | n # 6 of 10 ( Start time: 12:07:52 PM, 09 August 2020 ) |  |
|                          | is/are example(s) of synchronous communication.         |  |
|                          |   |  |
|                          |   |  |
|                          |   |  |
| Select th                | ne correct option                                       |  |
|                          | Register to Register                                    |  |
|                          |   |  |
|                          |   |  |
|                          | Register to Memory                                      |  |
| 0                        |   |  |
|                          | <u> </u>  |  |
|                          | Memory to Memory  |  |
| 0                        |   |  |
|                          | All of the given  |  |
| 0                        |   |  |
|                          |   |  |
|                          |   |  |

| CS501:9   | Semester Quiz # 01 Q                                       | uiz |
|-----------|--|-----|
| Question  | n # 7 of 10 ( Start time: 12:08:05 PM, 09 August 2020 )    |     |
| Taking o  | control of the system bus for a few bus cycles is known as |     |
|           |  |     |
|           |  |     |
| Select th | he correct option  |     |
|           | Bus Stealing   |     |
| 0         |  |     |
|           | Cycle Stealing   |     |
|           |  |     |
|           | Cycle Transfering  |     |
| 0         |  |     |
|           | None of given  |     |
| 0         |  |     |
|           |  |     |
|           |  |     |

| CS501:    | Semester Quiz # 01 Quiz Start Time: 12                                    |
|-----------|---|
| Question  | n # 8 of 10 ( Start time: 12:08:20 PM, 09 August 2020 )                   |
| In a prin | ter with DB-25 interface, signal is is better for edge triggered systems. |
|           |   |
|           |   |
|           |   |
| Select th | ne correct option   |
|           | BUSY#   |
| 0         |   |
|           | <b>2</b>  |
| 0         | PE#   |
|           |   |
|           | ACKNLG#   |
|           |   |
|           |   |
|           | STROB#  |
| O         |   |
|           |   |
|           |   |

| CS501:           | Semester Quiz # 01   | Quiz Start |
|------------------|--|------------|
|                  |  |            |
| Questio          | n # 9 of 10 ( Start time: 12:08:37 PM, 09 August 2020 )  |            |
| For inputhe data | t ports, the incoming data should be placed on bus only during the I/O read bus cycle. For this purpose, | are used.  |
| Select t         | ne correct option  |            |
| 0                | Flip Flops   |            |
|                  | Tri-state Buffers  |            |
| 0                | AND Gates  |            |
| 0                | Registers  |            |
|                  |  |            |

| CS501:    | Semester Quiz # 01 Quiz Start  |
|-----------|--|
| Question  | n # 10 of 10 ( Start time: 12:08:54 PM, 09 August 2020 )                       |
| How ca    | n you define an interrupt?   |
| Select ti | he correct option  |
|           | A process where an extern ce can speedup the working of the microprocessor     |
| 0         |  |
| 0         | A process where memor, can speed up programs execution speed                   |
|           | A process where an external device can get the attention of the microprocessor |
| 0         | A process where input devices can takeover the working of the microprocessor   |

## 2<sup>nd</sup> account

| CS501:    | Semester Quiz # 01                                      |
|-----------|---|
|           |   |
|           | n # 1 of 10 ( Start time: 12:20:08 PM, 09 August 2020 ) |
| ET =      |   |
|           |   |
|           |   |
|           |   |
|           |   |
| Select th | he correct option                                       |
|           | CPxICxT   |
| 0         |   |
|           |   |
|           | CPIxICxT  |
|           | \   |
|           |   |
|           | CPI / IC x T  |
| 0         | \   |
|           |   |
|           | CPI x IC / T  |
| 0         |   |
|           |   |
|           |   |
|           |   |

| 25501:5   | emester Quiz # 01  | Quiz Start Time: 12:2 |
|-----------|--|-----------------------|
|           | # 2 of 10 ( Start time: 12:20:59 PM, 09 August 2020 )                      |                       |
| In 8086/8 | 3088 processor, interrupt vector table is located at the memory location _ |                       |
|           |  |                       |
|           |  |                       |
|           |  |                       |
| Select th | e correct option   |                       |
|           |  |                       |
|           |  |                       |
|           | 4  |                       |
| 0         |  |                       |
|           |  |                       |
|           | 256  |                       |
| 0         |  |                       |
|           | 1001   |                       |
|           | 1024   |                       |
| 0         |  |                       |
|           |  |                       |
|           |  |                       |
|           |  |                       |

| C8501:                 | Semester Quiz # 01   | Quiz Start |
|------------------------|--|------------|
|                        | # 3 of 10 ( Start time: 12:21:20 PM, 09 August 2020 )          |            |
| Every tir<br>This is a | ne you press a key, an interrupt is generated.<br>n example of |            |
|                        |  |            |
| Select th              | e correct option   |            |
| _                      | Hardware interrupt   |            |
|                        |  |            |
|                        | Software interrupt   |            |
| 0                      |  |            |
|                        | All of the given   |            |
| 0                      |  |            |
|                        | None of the given  |            |
| 0                      | Troile of the given  |            |
|                        |  |            |

|         | # 4 of 10 ( Start time: 12:21     |                  |                    | ,     |
|---------|-----------------------------------|------------------|--------------------|-------|
| ost pa  | rallel I/O ports used with periph | ieral devices ar | e mapped on a rang | ge of |
|         |                                   |                  |                    |       |
|         |                                   |                  | Tr.                |       |
| lect ti | Bus addresses                     | 2                |                    |       |
| 0       | Dus addresses                     |                  |                    |       |
| 0       | Direct memory Access              |                  |                    |       |
|         | contiguous addresses              |                  |                    |       |
| 0       | Cache                             |                  |                    |       |
|         | "                                 |                  |                    |       |
|         |                                   |                  |                    |       |
|         |                                   |                  |                    |       |

| th is the last instruction of the ISR that is to be executed when the ISR terminates?  IRC  INT  | ct the correct option  IRET  IRQ  INT | ct the correct option  IRET  IRQ  INT | the correct option  IRET  INT | IRQ INT  |  |
|--|---------------------------------------|---------------------------------------|-------------------------------|----------|--|
| IRET  IRQ  INT   | IRQ INT                               | IRQ INT                               | IRQ INT                       | IRQ INT  |  |
| IRET  IRQ  INT   | IRQ INT                               | IRQ INT                               | IRQ INT                       | IRQ INT  |  |
| IRQ INT  | IRQ<br>INT                            | IRQ<br>INT                            | IRQ INT                       | IRQ INT  |  |
| INT STATE OF THE PROPERTY OF T | INT INT                               | INT INT                               | INT                           | D INT    |  |
| <b>\</b>   | <b>\</b>                              | <b>\</b>                              | <b>\</b>                      | <b>\</b> |  |
| NMI  | NMI                                   | NMI                                   | NMI                           | NMI      |  |
|  |                                       |                                       |                               |          |  |
|  |                                       |                                       |                               |          |  |
|  |                                       |                                       |                               |          |  |
|  |                                       |                                       |                               |          |  |

| CS501:    | Semester Quiz # 01 Quiz Start Time: 12:  |
|-----------|--|
| Question  | n # 6 of 10 ( Start time: 12:22:22 PM, 09 August 2020 )                        |
| How car   | n you define an interrupt?   |
| Select th | ne correct option  |
| 0         | A process where an external device can adup the working of the microprocessor  |
| 0         | A process where memory can speed up programs execution speed                   |
|           | A process where an external device can get the attention of the microprocessor |
| 0         | A process where input devices can takeover the working of the microprocessor   |
|           |  |

| S501:    | Semester Quiz # 01   | Quiz Start Time: 12: |
|----------|--|----------------------|
| Questio  | n # 7 of 10 ( Start time: 12:22:40 PM, 09 August 2020 )                |                      |
| A softw  | are routine performed when an interrupt is received by the computer is | called as            |
|          |  |                      |
| Select t | he correct option  |                      |
| 0        | Interrupt  |                      |
|          | Interrupt handler  |                      |
| 0        | Exception  |                      |
| 0        | Тгар   |                      |

| CS501:5   | Semester Quiz # 01 Quiz Start Tim                     |
|-----------|---|
| Question  | # 8 of 10 ( Start time: 12:23:00 PM, 09 August 2020 ) |
|           | A is faster than Programmer I/O technique because?    |
|           |   |
|           |   |
| Select th | e correct option                                      |
|           | DMA transfers data directly using CPU.                |
| 0         |   |
|           | DMA transfers data directly with tuying CPU           |
|           |   |
|           | DMA uses buffers with CPU                             |
| 0         |   |
|           | DMA uses interrupted driven I/O                       |
| 0         |   |
|           | Click to Save Answer 8                                |
|           |   |

| Radix Compliment  Diminished Radix Compliment  Signed Magnitude Form | x <sup>c</sup> = (b <sup>m</sup> - x)mod b <sup>m</sup> act the correct option  Radix Compliment  Diminished Radix Compliment  Signed Magnitude Form | x <sup>c</sup> = (b <sup>m</sup> - x)mod b <sup>m</sup> cot the correct option  Radix Compliment  Diminished Radix Compliment  Signed Magnitude Form | x <sup>c</sup> = (b <sup>m</sup> - x)mod b <sup>m</sup> act the correct option  Radix Compliment  Diminished Radix Compliment  Signed Magnitude Form | stior    | n # 9 of 10 ( Start time: 12:23:16 PM, 09 August 2020 ) |                    |
|--|--|--|--|----------|---|--------------------|
| Radix Compliment  Diminished Radix Compliment  Signed Magnitude Form | Radix Compliment  Diminished Radix Compliment  Signed Magnitude Form   | Radix Compliment  Diminished Radix Compliment  Signed Magnitude Form   | Radix Compliment  Diminished Radix Compliment  Signed Magnitude Form   | ven a    |   |                    |
| Padix Compliment  Diminished Radix Compliment  Signed Magnitude Form | Diminished Radix Compliment  Signed Magnitude Form   | Diminished Radix Compliment  Signed Magnitude Form   | Diminished Radix Compliment  Signed Magnitude Form   |          | $\mathbf{x}^c = (\mathbf{b}^m - \mathbf{x})\mathbf{n}$  | nod b <sup>m</sup> |
| O Diminished Radix Compliment O Signed Magnitude Form                | Diminished Radix Compliment  Signed Magnitude Form   | Diminished Radix Compliment  Signed Magnitude Form   | Diminished Radix Compliment  Signed Magnitude Form   | elect th | ne correct option                                       |                    |
| O Signed Magnitude Form  | Signed Magnitude Form  | O Signed Magnitude Form  | Signed Magnitude Form  |          | Radix Compliment  |                    |
| 0  |  | O \  |  | 0        | Diminished Radix Compliment                             |                    |
| Biased Representation  | Biased Representation  | Biased Representation  | Biased Representation  | 0        | Signed Magnitude Form                                   |                    |
|  |  |  |  | 0        | Biased Representation                                   |                    |
|  |  |  |  |          |   |                    |
|  |  |  |  |          |   |                    |
|  |  |  |  |          |   |                    |

| CS501:S   | Semester Quiz # 01   | Quiz Start Time: |
|-----------|--|------------------|
| Question  | # 10 of 10 ( Start time: 12:23:35 PM, 09 August 2020 )               |                  |
| How doe   | s DMA saves CPU time?  |                  |
|           |  |                  |
|           |  |                  |
| Select th | e correct option   |                  |
|           | By controlling data transfer between I/O levice and memory directly. |                  |
|           |  |                  |
|           | By storing all data in a buffer of ater transferred to the CPU.      |                  |
| 0         |  |                  |
|           | By periodically polling.   |                  |
| 0         |  |                  |
|           | By issuing an interrupt request to the CPU to request attention.     |                  |
| 0         |  |                  |

## 3<sup>rd</sup> account

| CS501:   | Semester Quiz # 01 Qu                                   |
|----------|---|
| Questio  | n # 1 of 10 ( Start time: 12:26:20 PM, 09 August 2020 ) |
| Select t | he parts of a hard disk.                                |
|          |   |
| Select t | he correct option                                       |
| 0        | Header only   |
| 0        | Data section and a trailer                              |
| 0        | Data section only                                       |
|          | Header, data section and a trailer.                     |
|          |   |

| estion # 2 of 10 ( Start time: 12:26:37 PM, 09 August 2020 )  ect the correct option  Programmed I/O  Interrupt driven I/O  Direct memory access(DMA) | estion # 2 of 10 ( Start time: 12:26:37 PM, 09 August 2020 )                          | estion # 2 of 10 ( Start time: 12:26:37 PM, 09 August 2020 )  | ect the correct option  Programmed I/O  Interrupt driven I/O  Direct memory access(DMA) | S501:   | Semester Quiz # 01 Quiz Start Tin  | ne |
|---|---|---|---|---------|--|----|
| ect the correct option Programmed I/O Interrupt driven I/O Direct memory access(DMA)  | lect the correct option Programmed I/O Interrupt driven I/O Direct memory access(DMA) | allows a peripheral to read and write memory without intervention by the CPU.  lect the correct option  Programmed I/O  Interrupt driven I/O  Direct memory access(DMA) | ect the correct option Programmed I/O Interrupt driven I/O Direct memory access(DMA)    | 0001.   | Guiz otati in  |    |
| ect the correct option Programmed I/O Interrupt driven I/O Direct memory access(DMA)  | lect the correct option Programmed I/O Interrupt driven I/O Direct memory access(DMA) | lect the correct option Programmed I/O Interrupt driven I/O Direct memory access(DMA)   | ect the correct option  Programmed I/O  Interrupt driven I/O  Direct memory access(DMA) |         |  |    |
| O Interrupt driven I/O Direct memory access(DMA)  | O Interrupt driven I/O  Direct memory access(DMA)                                     | O Interrupt driven I/O  Direct memory access(DMA)   | Programmed I/O  Interrupt driven I/O  Direct memory access(DMA)                         |         | allows a periprieral to read and write memory without intervention by the CPO. |    |
| O Interrupt driven I/O  Direct memory access(DMA)   | O Interrupt driven I/O Direct memory access(DMA)                                      | O Interrupt driven I/O Direct memory access(DMA)  | Interrupt driven I/O  Direct memory access(DMA)   | elect t | ne correct option  |    |
| Direct memory access(DMA)   | Direct memory access(DMA)   | Direct memory access(DMA)   | Direct memory access(DMA)   | 0       | Programmed I/O   |    |
|   |   |   |   | 0       | Interrupt driven I/O   |    |
| OPolling  | Polling   | Polling   | Polling   |         | Direct memory access(DMA)  |    |
|   |   |   |   | 0       | Polling  |    |
|   |   |   |   |         |  |    |
|   |   |   |   |         |  |    |
|   |   |   |   |         |  |    |
|   |   |   |   |         |  |    |
|   |   |   |   |         |  |    |
|   |   |   |   |         |  |    |

| CS501:    | Semester Quiz # 01 Qu   | iiz Start Tin |
|-----------|---|---------------|
| Question  | n # 3 of 10 ( Start time: 12:26:54 PM, 09 August 2020 )               |               |
| The Per   | ntium does allow the use of some part of its accumulator register EAX |               |
|           |   |               |
| Select th | ne correct option   |               |
| 0         | 8 bits  |               |
| 0         | 16 bits   |               |
|           | 32 bits   |               |
| 0         | 64 bits   |               |
|           |   |               |

|                    | Semester Quiz # 01   | Quiz Start Time: 12 |
|--------------------|--|---------------------|
|                    | n # 4 of 10 ( Start time: 12:27:07 PM, 09 August 2020 )                      |                     |
| or inpu<br>he data | It ports, the incoming data should be placed on bus cycle. For this purpose, | are used.           |
|                    |  |                     |
|                    |  |                     |
|                    |  |                     |
|                    |  |                     |
| elect ti           | ne correct option  |                     |
|                    | Flip Flops   |                     |
| 0                  |  |                     |
|                    |  |                     |
|                    | Tri-state Buffers  |                     |
|                    |  |                     |
|                    |  |                     |
|                    | AND Gates  |                     |
| 0                  |  |                     |
| 0                  |  |                     |
|                    | Ponistore  |                     |
| _                  | Registers  |                     |
| 0                  |  |                     |
|                    | II   |                     |

| CS501:Semester Quiz # 01   | Quiz Start Time: 12:26 PM, 09 August 20 |
|--|---|
| uestion # 5 of 10 ( Start time: 12:27:26 PM, 09 August 2020 )    | ) Total Mark                            |
| A component connected to the system bus and having control of it | during a particular bus cycle is called |
|  |   |
|  |   |
|  |   |
| elect the correct option   |   |
| Slave component  |   |
|  |   |
| Master component   |   |
|  |   |
| System bus   |   |
| 0  |   |
| D.#  |   |
| Buffer component   |   |
|  |   |
|  |   |
|  |   |
|  |   |
|  |   |
|  |   |
|  |   |
|  |   |
|  |   |
|  |   |
|  |   |
|  |   |
|  |   |

| CS501:Semester Quiz # 01 Quiz Start Time: 12:26 PM, 09 A |   |         |
|--|---|---------|
| _  | n # 6 of 10 ( Start time: 12:27:44 PM, 09 August 2020 )   | Total M |
| Which I  | O technique will be used by a sound card that may need to access data stored in the computer's RAM? |         |
| Select ti  | ne correct option   |         |
| 0  | Programmed I/O  |         |
| 0  | Interrupt driven I/O  |         |
|  | Direct memory access(DMA)   |         |
| 0  | Polling   |         |
|  |   |         |

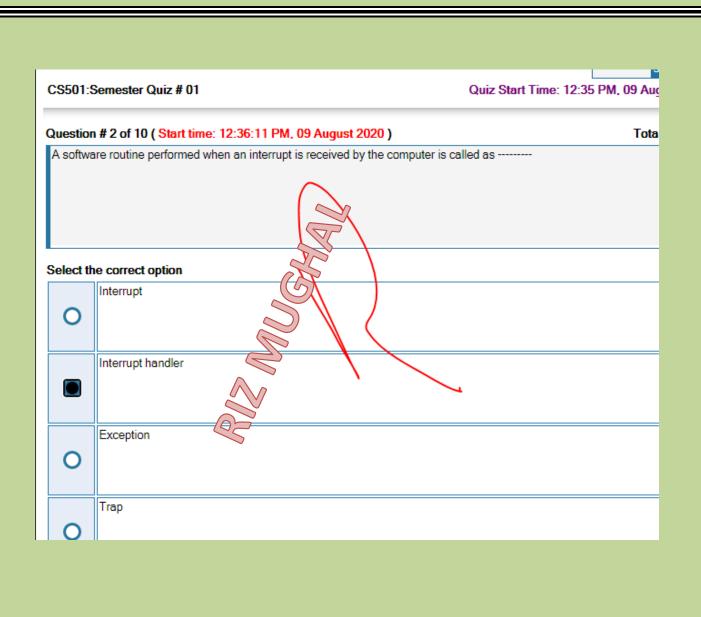
| CS501:Semester Quiz # 01   | Quiz Start Time: 12:26 PM, 09 August 2020                        |
|--|--|
| Question # 7 of 10 ( Start time: 12:28:01 PM, 09 August 202                  | O) Total Marks: 1  |
| In the little-endian format exchanging data between computers, by the other. | the data transmitted by one will be received in a "swapped" form |
| Select the correct option  | ***  |
| Organized  | //   |
| O Signals  | //   |
| Swapped  | //   |
| O Arranged   | //   |

| CS501:Semester Quiz # 01                | Quiz S   | Start Time: 12:26 PM, 09 August 202 |
|---|--|-------------------------------------|
| Question # 8 of 10 ( Start time: 12     |  | Total Marks:                        |
| A computer interface is an<br>connected | circuit that matches the requirements of the two | subsystems between which it is      |
| Select the correct option               |  |                                     |
| Digital                                 |  | <i>/</i> -                          |
| Electronic                              |  |                                     |
| Primary                                 |  | <i>/</i> -                          |
| Obituary                                |  | <i>h</i>                            |
|   |  |                                     |
|   |  |                                     |
|   |  |                                     |
|   |  |                                     |
|   |  |                                     |

| estion # 9 of 10 (Start time: 12:28:35 PM, 09 Auguments one of the following methods for resolving the p | rity, the device with the highest priority is placed in the first position, |
|--|---|
| llowed by lower-priority devices up to the device with the   | lowest priority, which is placed last in the series?                        |
|  |   |
| lect the correct option  |   |
| Asynchronous   |   |
| 0  | <i>/</i> /  |
| Daisy-Chaining Priority  |   |
|  | 11  |
| Parallel   |   |
| 0  | //  |
| Semi-synchronous   |   |
| 0  | //  |
|  |   |
|  |   |
|  |   |
|  |   |

| CS501:    | Semester Quiz # 01  | Quiz Start Time: 12:26 PM, 09 August 2020 |
|-----------|---|---|
| Question  | n # 10 of 10 ( Start time: 12:28:52 PM, 09 August 2020 )                | Total Marks:                              |
| Every in  | sterrupt handler has an interrupt return (IRET) instruction, this instr | uction is an example of return.           |
| Select th | ne correct option   | /   |
| Coloct ti | NEAR  |   |
| 0         |   | //  |
|           | FAR   |   |
|           |   | //  |
|           | SHORT   |   |
| 0         |   | //  |
|           | RELATIVE  |   |
| 0         |   | <i>/</i> -                                |

4<sup>th</sup> account



| CS501:Semeste                           | er Quiz # 01 Quiz Start   | t Time: 12:35 PM, 09 August |
|---|---|-----------------------------|
| Question # 3 of                         | 10 ( Start time: 12:36:29 PM, 09 August 2020 )  | Total Ma                    |
| Identify the follov<br>"The prior chara | wing type of serial communication error condition:<br>cter that was received was not still read by the CPU and is over written by a | new received character."    |
|   |   |                             |
| Select the corre                        | ct option C   |                             |
| O Framin                                | g error   |                             |
| O Parity 6                              | error   |                             |
| Overrui                                 | n error   |                             |
| Under-                                  | run error   |                             |

| CS501:   | CS501:Semester Quiz # 01 Quiz Start Time: 12:3                 |                              |  |  |  |
|----------|--|------------------------------|--|--|--|
|          | Question # 4 of 10 ( Start time: 12:36:47 PM, 09 August 2020 ) |                              |  |  |  |
| Taking   | control of the system bus for                                  | a few bus cycles is known as |  |  |  |
|          |  |                              |  |  |  |
| Select t | he correct option  |                              |  |  |  |
| 0        | Bus Stealing   |                              |  |  |  |
|          | Cycle Stealing   |                              |  |  |  |
| 0        | Cycle Transfering  |                              |  |  |  |
| 0        | None of given  |                              |  |  |  |

| CS501:    | Semester Quiz # 01 Quiz Start Time: 12:35 PN   |
|-----------|--|
| Question  | n # 5 of 10 ( Start time: 12:37:01 PM, 09 August 2020 )                                  |
| What is   | the status of the ACKNLG# signal when a character is completely received by the printer? |
|           |  |
| Select th | he correct option  |
|           | It goes from low to high   |
| 0         |  |
|           | It goes from high to low   |
|           | It toggles its state   |
| 0         |  |
|           | It remains unaffected  |
| 0         |  |
|           |  |

|          | Semester Quiz # 01 Quiz Start Time: 12:35 PM, 09                                  |
|----------|---|
|          | n # 6 of 10 ( Start time: 12:37:16 PM, 09 August 2020 )                           |
| How ca   | n you define an interrupt?  |
|          |   |
| elect ti | ne correct option   |
| 0        | A process where an external device can specific the working of the microprocessor |
| 0        | A process where memory can speed to programs execution speed                      |
|          | A process where an external device can get the attention of the microprocessor    |
| 0        | A process where input devices can takeover the working of the microprocessor      |

| CS501:S   | CS501:Semester Quiz # 01 Quiz Star  |  |  |
|-----------|---|--|--|
|           | # 7 of 10 ( Start time: 12:38:45 PM, 09 August 2020 )                           |  |  |
| How Inte  | errupt driven I/O is better than polling because?                               |  |  |
|           |   |  |  |
| Select th | e correct option  |  |  |
| 0         | Interrupt driver I/O is easy to design  |  |  |
| 0         | Interrupt driver I/O is enhan of version of polling.                            |  |  |
|           | Interrupt driver I/O does not waste time on checking which device is available. |  |  |
| 0         | Interrupt driven I/O is easy to program.  |  |  |
|           |   |  |  |
|           |   |  |  |

| CS501:    | Semester Quiz # 01   | Quiz Start Time: 12:35 PM, 09 |
|-----------|--|-------------------------------|
| Question  | n # 8 of 10 ( Start time: 12:39:08 PM, 09 August 2020 )  | т                             |
| For inpu  | ut ports, the incoming data should be placed on<br>a bus only during the I/O read bus cycle. For this purpose, | are used.                     |
|           |  |                               |
| Select th | he correct option  |                               |
| 0         | Flip Flops   |                               |
|           | Tri-state Buffers  | •                             |
| 0         | AND Gates  |                               |
| 0         | Registers  |                               |
|           |  |                               |

|          |   | t Time: 12:35 PM, 09 August 2020                    |
|----------|---|---|
|          | n # 9 of 10 (Start time: 12:39:27 PM, 09 August 2020)  tle-endian format exchanging data between computers, the data transmitted by one wither. | Total Marks: 1 vill be received in a "swapped" form |
| elect th | ne correct option   |   |
| 0        | Organized   | 11  |
| 0        | Signals   | 11  |
|          | Swapped   |   |
| 0        | Arranged  | 11  |

| CS501:S   | Semester Quiz # 01  | Quiz Start Time: 12:35 PM, 09 August |
|-----------|---|--------------------------------------|
| Question  | # 10 of 10 ( Start time: 12:39:49 PM, 09 August 2020 )                | Total Ma                             |
| Which I/  | O technique will be used by a sound card that may need to access data | stored in the computer's RAM?        |
|           |   |                                      |
| Select th | e correct option  |                                      |
| 0         | Programmed I/O  |                                      |
| 0         | Interrupt driven I/O  |                                      |
|           | Direct memory access(DMA)   |                                      |
| 0         | Polling   |                                      |

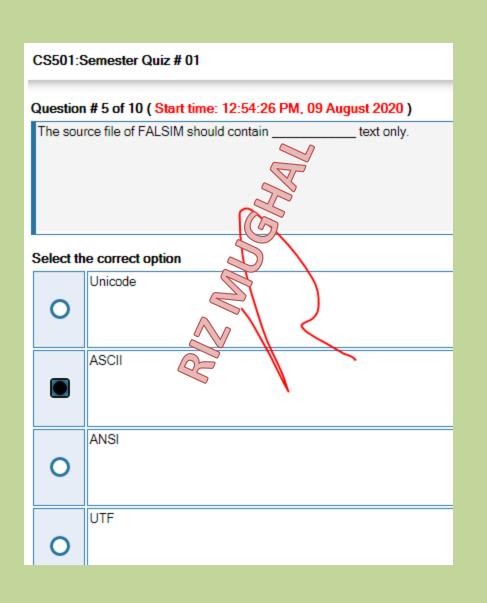
## 5<sup>th</sup> account

| CS501:S   | Semester Quiz # 01  | Quiz Start Time: 12: |
|-----------|---|----------------------|
| Question  | # 1 of 10 ( Start time: 12:53:10 PM, 09 August 2020 )         |                      |
| Along w   | th information bits we add up another bit which is called the | bit.                 |
| Select th | e correct option  |                      |
| 0         | CRC   |                      |
| 0         | Hamming   |                      |
| 0         | Error Detection   |                      |
|           | Parity  |                      |
|           |   |                      |

| CS501:9   | Semester Quiz # 01  |
|-----------|---|
|           | #0 f40 f0; es 40 50 00 PM 00 A  |
|           | n # 2 of 10 ( Start time: 12:53:36 PM, 09 August 2020 ) buffers are used for removing |
| TIT State | bullets are used for removing   |
|           |   |
|           | 58  |
|           |   |
| Select th | ne correct option   |
|           | Instruction collision   |
| 0         |   |
|           |   |
|           | bus collision   |
| 0         |   |
|           |   |
|           | Instruction contention  |
| 0         |   |
|           | bus contention  |
|           | Dus Contention  |
|           |   |
|           |   |
|           |   |

| S501:    | Semester Quiz # 01   | Quiz Start Time: 12:53 PM, 09 Aug   |
|----------|--|-------------------------------------|
|          | n # 3 of 10 ( Start time: 12:53:49 PM, 09 August 2020 )            | Total                               |
| n which  | n technique does the hardware directly access host memory for read | ling or writing independent of CPU? |
| elect ti | he correct option  |                                     |
|          | Direct Memory Access (DMA)   |                                     |
| 0        | Programmed I/O   |                                     |
| 0        | Interrupt driven I/O   |                                     |
| 0        | Polling  |                                     |
|          |  |                                     |
|          |  |                                     |
|          |  |                                     |
|          |  |                                     |
|          |  |                                     |
|          |  |                                     |

| Question # 4 of 10 ( Start time: 12:54:12 PM, 09 August 2020 )  The main issue/s in error control is/are  Select the correct option  Detection of Error  Correction of Error  Both Detection of Error and Correction of Error  Avoidance of Error | CS501:5   | Semester Quiz # 01                                      | Qı |
|---|-----------|---|----|
| Select the correct option  Detection of Error  Correction of Error  Both Detection of Error and Correction of Error  Avoidance of Error   | Question  | n # 4 of 10 ( Start time: 12:54:12 PM, 09 August 2020 ) |    |
| O Correction of Error  Both Detection of Error and Correction of Error  Avoidance of Error  | The mai   | n issue/s in error control is/are                       |    |
| O Correction of Error  Both Detection of Error and Correction of Error  Avoidance of Error  |           |   |    |
| O Correction of Error  Both Detection of Error and Correction of Error  Avoidance of Error  |           |   |    |
| Correction of Error  Both Detection of Error and Correction of Error  Avoidance of Error  | Select th | ne correct option                                       |    |
| Correction of Error  Both Detection of Error and Correction of Error  Avoidance of Error  |           | Detection of Error                                      |    |
| Both Detection of Error and Correction of Error  Avoidance of Error   |           |   |    |
| Both Detection of Error and Correction of Error  Avoidance of Error   |           | Correction of Error                                     |    |
| Avoidance of Error  |           |   |    |
| Avoidance of Error  |           | Both Detection of Error and Correction of Error         |    |
|   |           |   |    |
| 0   |           | Avoidance of Error                                      |    |
|   | 0         |   |    |



| CS501:S   | Semester Quiz # 01                                    |
|-----------|---|
| Question  | # 6 of 10 ( Start time: 12:54:41 PM, 09 August 2020 ) |
| The dire  | ctive is used to define variables.                    |
| Select th | e correct option                                      |
|           | .equ  |
| 0         | .db   |
| 0         | .sw   |
| 0         | .org  |
|           |   |

## CS501:Semester Quiz # 01 Question # 7 of 10 ( Start time: 12:54:58 PM, 09 August 2020 ) human works with base 10 and computers work with base \_\_ Select the correct option 10 16

| CS501:Semester     | Quiz # 01   | Quiz Start Time: 12                | 2:53 PM, 09 August 202 |
|--------------------|---|------------------------------------|------------------------|
|                    | ( Start time: 12:55:13 PM, 09 August 2020           |                                    | Total Marks:           |
| The information ab | out interrupt vector is given in 8-bits, from bit 0 | ) to 7, which is translated to bit | on the data bus.       |
|                    |   |                                    |                        |
| Select the correct | option  | V                                  |                        |
| 16 to 23           |   |                                    | <i>h</i>               |
| O 11 to 18         |   |                                    | <i>1</i> ,             |
| O to 7             |   |                                    | 1.                     |
| 8 to 15            |   |                                    | 11                     |
|                    |   |                                    |                        |
|                    |   |                                    |                        |
|                    |   |                                    |                        |
|                    |   |                                    |                        |
|                    |   |                                    |                        |
|                    |   |                                    |                        |
|                    |   |                                    |                        |
|                    |   |                                    |                        |
|                    |   |                                    |                        |

| pestion # 9 of 10 ( Start time: 12:55:32 PM, 09 August 2020 )  the can be determined from the number of platters and the number of tracks.  Pelect the correct option  Speed of processing  execution time  storage capacity  Latency | elect the correct option  Speed of processing  execution time  storage capacity  Latency | elect the correct option  Speed of processing  execution time  storage capacity  Latency | elect the correct option  Speed of processing  execution time  storage capacity  Latency | elect the correct option  Speed of processing  execution time  storage capacity  Latency | elect the correct option  Speed of processing  execution time  storage capacity  Latency | ect the correct option  Speed of processing  execution time  storage capacity |  |
|---|--|--|--|--|--|---|--|
| elect the correct option  Speed of processing  execution time  storage capacity  Latency  | elect the correct option  Speed of processing  execution time  storage capacity  Latency | elect the correct option  Speed of processing  execution time  storage capacity  Latency | elect the correct option  Speed of processing  execution time  storage capacity  Latency | elect the correct option  Speed of processing  execution time  storage capacity  Latency | elect the correct option  Speed of processing  execution time  storage capacity  Latency | ect the correct option  Speed of processing  execution time  storage capacity |  |
| Speed of processing  execution time  storage capacity  Latency  | Speed of processing  execution time  storage capacity  Latency                           | Speed of processing  execution time  storage capacity  Latency                           | Speed of processing  execution time  storage capacity  Latency                           | Speed of processing  execution time  storage capacity  Latency                           | Speed of processing  execution time  storage capacity  Latency                           | execution time  storage capacity  |  |
| Speed of processing  execution time  storage capacity  Latency  | Speed of processing  execution time  storage capacity  Latency                           | Speed of processing  execution time  storage capacity  Latency                           | Speed of processing  execution time  storage capacity  Latency                           | execution time storage capacity  Latency   | Speed of processing  execution time  storage capacity  Latency                           | execution time  storage capacity  |  |
| execution time  storage capacity  Latency   | execution time  storage capacity  Latency  | execution time  storage capacity  Latency  | execution time storage capacity  Latency   | execution time storage capacity  Latency   | execution time storage capacity  Latency   | execution time storage capacity   |  |
| Storage capacity  Latency   | storage capacity  Latency  | storage capacity  Latency  | storage capacity  Latency  | storage capacity  Latency  | storage capacity  Latency  | storage capacity  |  |
| Latency   | Latency  | Latency  | Latency  | Latency  | Latency  |   |  |
|   |  |  |  |  |  |   |  |
|   |  |  |  |  |  |   |  |
|   |  |  |  |  |  |   |  |
|   |  |  |  |  |  |   |  |
|   |  |  |  |  |  |   |  |

|          | on # 10 of 10 ( Start time: 12:55:48 PM, 09 August 2020 )  Inversion of numbers from a representation in one base to another is known as |
|----------|--|
|          |  |
| Select t | the correct option   |
|          | Radix Conversion   |
| 0        | Number Representation  |
| 0        | Decimal representation   |
| 0        | Hexadecimal Representation   |
|          |  |