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| 1. | The shift logical right operation inserts |
|-----|--|
| 2. | After the execution of "PUSH AX" statement |
| 3. | The extended ASCII has 256 characters |
| 4. | The iAPX88 processor supportsmodes of memory access. |
| 5. | In STOS instruction, the implied source will always be in AL or AX registers |
| 6. | The maximum memory, IAPX88 can access is |
| 7. | The registers IP, SP, BP, SI, DI, and BX all can contain aoffset. |
| 8. | In the "mov ax, 5" 5 is the operand. |
| 9. | In MUL instruction if the source operand is a word then it is multiplied by register |
| 10. | The prevalent and standard format for representation of characters in computers is |
| 11. | which bit sets the character "blinking" on the screen? |
| 12. | "mov byte [num1], 5" is instruction. |
| 13. | can process blocks of data in one go. |
| 14. | In string instructions, CX is always |
| 15. | STOS transfers a byte or word from register AL or AX to the string element addressed by |
| 16. | The execution of the instruction "mov word [ES:0], 0x0741" will print character "A" on |
| | screen, color of the character will be |
| 17. | In A4FB:4872 Segment:offset pair the physical address is (both segment and offset are in |
| | hexadecimal): A9822 |
| | Which of the following operations relating to PUSH is true? |
| 19. | If the decimal number "35" is shifted by two bits to left, the new value will be |

21. Explain the fuction of rotate right (ROR) instruction

20. Which of the following flags will be affected by MOVSB?

The rotate right (ROR) and rotate through carry right (RCR) instructions shift all the bits toward less significant bit positions, except for the least-significant bit, which is rotated to the most-significant bit location

22. Why REP prefix is generally not used with LODS instruction?

The lods instruction is unique among the string instructions. We will never use a repeat prefix with this instruction. Because it copies the byte or word pointed at by ds:si into the al, ax, or eax register, after which it increments or decrements the si register by one, two, or four. Repeating this instruction via the repeat prefix would serve no purpose whatsoever since the accumulator register will be overwritten each time the lods instruction repeats. At the end of the repeat operation, the accumulator will contain the last value read from memory.

23. Write all steps of algorithm for printing number 352.

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In this technique the first digit printed is the right most one

Divide the number by base (10 in case of decimal).. The remainder after

first division was 3, after second division was 5 and after the third division

was 2.

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- The remainder is its right most digit
- Convert the digit to its ASCII representation
- Save this digit on stack
- If the quotient is non-zero repeat the whole process to get the next digit, otherwise stop.
- Pop digits one by one and print on screen left to right. Stack is a Last In First Out structure so if 3, 5, and 2 are pushed on it, 2, 5, and 3 will come

out in this order.

24. What are the result after performing the instruction (each carry 1 marks)

- 1. and ax,bx
- 2. or ax,bx
- 3. xor ax,bx

Given that ax = 00110011 and bx = 00010001

25. Describe Local Variables?

A local variable is valid within the statement block in which it is defined and within any nested statement blocks, unless you redefine the variable within the statement block.

Local variables should be created when the subroutine is called and discarded afterwards. So that the spaced used by them can be reused for the local variables of another subroutine. They only have meaning inside the subroutine and no meaning outside it.

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It is important role of the stack to create local variables that are only needed while the subroutine is in execution and not afterwards. They should not take permanent space like global variables.

The most convenient place to store these variables is the stack. We need some special manipulation of the stack for this task. We need to produce a gap in the stack for our variables.

Are valid only for the duration of the SPL routine

Are reset to their initial values or to a value the user passes to the routine, each time the routine is executed

Cannot have default values

26. Explain the complete operation of Interrupt when it is generated.

Interrupt is the result of an INT instruction (software interrupt) or it is generated by an external hardware which passes the interrupt number by a different mechanism. The currently executing instruction is completed, the current value of FLAGS is pushed on the stack, then the current code segment is pushed, then the offset of the next instruction is pushed. After this it automatically clears the trap flag and the interrupt flag to disallow further interrupts until the current routine finishes. After this it loads the word at nx4 in IP and the word at nx4+2 in CS if interrupt n was generated. As soon as these values are loaded in CS and IP execution goes to the start of the interrupt handler. When the handler finishes its work it uses the IRET instruction to return to the caller. IRET pops IP, then CS, and then FLAGS. The original value of IF and TF is restored which re-enables further interrupts

Stack is a _____ that behaves in a first in last out manner.

- Program
- data structure
- Heap
- None of the Given

The physical address of the stack is obtained by

- SS:SI combination
- SS:SP combination
- ES:BP combination
- ES:SP combination

Foreground and background parameter will be

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- 32bits
- 16bits
- 8bits
- 4bits

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The clear screen operation initialize whole block of memory

- 0741
- 0417
- 0714
- 0174

In STOSB instruction, when DF is Set, SI is

- Incremented by 1
- Incremented by 2
- Decremented by 1 (Not confirmed)
- Decremented by 2

Assembly language is:

- Low-level programming language
- High-level programming language
- Also known as machine language
- Not considered closer to the computer

A 32 Bit processor has accumulator of ------

- 8 bit
- 16 bit
- <u>32 bit</u>
- 64 bit

To transfer control back the RET instruction take

- 1 argument
- 1 argument
- 3 arguments
- No arguments

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RET is executed, it recovers the values from

- Register
- Stack
- Data segment
- Code segment

To convert any digit to its ASCII representation

- Add 0x30 in the digit
- Subtract 0x30 from the digit
- Add 0x61 in the digit
- Subtract 0x61 from the digit

The prevalent convention in most high level languages is stack clearing by the

- <u>Caller</u>
- Callee
- <u>RET</u>
- Stack

After execution of JCXZ instruction CX will changed with flag affect.

- CF
- OF
- DF
- None of Above

Execution of the instruction "mov word [ES:0], 0x0741" will print

- "A" appear on the top left of screen
- "A" appear on the top right of screen
- "A" appear on the center of screen
- "A" appear on the bottom left of screen

if contains decimal -2 and BX contains decimal 2 then after the execution of instructions:

CMP AX, BX

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JA label

- Jump will be taken
- Zero flag will set
- ZF will contain value -4
- Jump will not be taken

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Which of the following options contain the set of instructions to open a window to the video memory?

- mov AX, 0xb008 mov ES, AX
- mov AX, 0xb800 mov ES, AX
- mov AX, 0x8b00 mov ES, AX
- mov AX, 0x800b mov ES, AX

If D is "35" is shift to left 2 bits the new value

- 35
- 70
- 140
- 17

Execution of the instruction "mov word [ES:0], 0x1230" will print the character color will

- Grean
- White
- Red
- Black

Q#21 Mark 2

What are the instructions used by assembly language for permanent and temporary diversions.

Q#22 Mark 2

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Which instruction is used to determine zero bit in string.

Q#23 Mark 3

Explain the use of TEST instruction.

The test instruction is used for bit testing. BX holds the mask and in every next iteration it is shifting left, as our concerned bit is now the next bit.

Q#24 Mark 3

Explain LES and LDS

The string instructions need source and destination in the form of a segment offset pair. LES and LDS load a segment register and a general purpose register from two consecutive memory locations. LES loads ES while LDS loads DS. Both instructions has two parameters, one is the general purpose register to be loaded and the other is the memory location from which to load these registers. The major application of these instructions is when a subroutine receives a segment offset pair as an argument and the pair is to be loaded in a segment and an offset register.

O#25 Mark 5

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Describe local variables.

Another important role of the stack is in the creation of local variables that are only needed while the subroutine is in execution and not afterwards. They should not take permanent space like global variables. Local variables should be created when the subroutine is called and discarded afterwards. So that the spaced used by them can be reused for the local variables of another subroutine. They only have meaning inside the subroutine and no meaning outside it.

The most convenient place to store these variables is the stack. We need some special manipulation of the stack for this task. We need to produce a gap in the stack for our variables. This is explained with the help of the swapflag in the bubble sort example.

The swapflag we have declared as a word occupying space permanently is only needed by the bubble sort subroutine and should be a local variable. Actually the variable was introduced with the intent of

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making it a local variable at this time. The stack pointer will be decremented by an extra two bytes thereby producing a gap in which a word can reside. This gap will be used for our temporary, local, or automatic variable; however we name it. We can decrement it as much as we want producing the desired space, however

the decrement must be by an even number, as the unit of stack operation is a word. In our case we needed just one word. Also the most convenient position for this gap is immediately after saving the value of SP in BP. So that the same base pointer can be used to access the local variables as well; this time using negative offsets. The standard way to start a subroutine which needs to access parameters and has local variables is as under.

push bp

mov bp, sp

sub sp, 2

The gap could have been created with a dummy push, but the subtraction makes it clear that the value pushed is not important and the gap will be used for our local variable. Also gap of any size can be created in a single instruction with subtraction. The parameters can still be accessed at bp+4 and bp+6 and the swapflag can be accessed at bp-2. The subtraction in SP was after taking the snapshot; therefore BP is above the parameters but below the local variables. The parameters are therefore accessed using

positive offsets from BP and the local variables are accessed using negative offsets.

Question No: 1 (Marks: 1) - Please choose one

To transfer control back the RET instruction take

- 1 argument http://www.vustudents.net
- 1 argument

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| • | 3 arguments | |
|---|-------------|--|
| • | No argument | S |
| | (| Question No: 2 (Marks: 1) - Please choose one |
| | lr | n STOSB instruction SI is decremented or incremented by |
| | | 4 |
| | | 1 |
| | | 2 |
| | | 3 |
| | (| Question No: 3 (Marks: 1) - Please choose one |
| | | MPS instruction subtracts the source location to ne destination location. Destination location always lies in |
| | | |
| | | DS:SI |
| | | DS:DI |
| | | ES:SI |

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ES:DI

Question No: 4 (Marks: 1) - Please choose one

Regarding assembler, which statement is true:

Assembler converts mnemonics to the corresponding OPCODE

- Assembler converts OPCODE to the corresponding mnemonics
- Assembler executes the assembly code all at once
- Assembler executes the assembly code step by step

Question No: 5 (Marks: 1) - Please choose one

If "BB" is the OPCODE of the instruction which states to "move a constant value to AX register", the hexadecimal representation (Using little Endian notation) of the instruction "Mov AX,336" ("150" in hexadecimal number system) will be:

0xBB0150

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| 0x5001BB | |
|-----------------------|--|
| 0x01BB50 | |
| 0xBB5001 | |
| Question No: 6 | (Marks: 1) - Please choose one |
| In the instruction MO | OV AX, 5 the number of operands are |
| | |
| 1 | |
| 2 | |
| 3 | |
| 4 | |
| Question No: 7 | (Marks: 1) - Please choose one |
| The maximum para | meters a subroutine can receive (with the help of registers) are |
| | |
| | |
| 6 | |
| 7 | |
| 8 | |
| 9 | |
| | |

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| Question No: 8 | (Marks: 1) - Please choose one | |
|--------------------------------|---|-----------|
| In assembly the C | X register is used normally as a | register. |
| | | |
| source | | |
| counter | | |
| index | | |
| pointer | | |
| | | |
| Question No: 9 | (Marks: 1) - Please choose one | |
| | | |
| All the addressing me address. | echanisms in iAPX 8 8 return a number called | |
| | | |
| | | |
| effective | | |
| faulty | | |
| indirect | | |
| direct | | |
| Question No: 10 | (Marks: 1) - Please choose one | |
| | | |
| When a 16 bit numb | per is divided by an 8 bit number, the dividend will be | e in |
| | | |
| _ | | |
| AX | | |
| ВХ | | |

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| CX | | | | |
|--|--|--|--|--|
| DX | | | | |
| | | | | |
| Question No: 11 | (Marks: 1) - Please choose one | | | |
| in Left-Shift-Opera | tion the left most bit | | | |
| | | | | |
| will drop | | | | |
| will go into | CF | | | |
| Will come to | Will come to the right most | | | |
| will be alwa | ys 1 | | | |
| | | | | |
| | | | | |
| Question No: 12 | (Marks: 1) - Please choose one | | | |
| Suppose the deci | (Marks: 1) - Please choose one mal number "35" after shifting its binary two v value becomes | | | |
| Suppose the deci | mal number "35" after shifting its binary two | | | |
| Suppose the decilor bits to left, the new | mal number "35" after shifting its binary two | | | |
| Suppose the decident bits to left, the new | mal number "35" after shifting its binary two | | | |
| Suppose the deciple bits to left, the new 35 | mal number "35" after shifting its binary two | | | |

When divide overflow occurs processor will be interrupted this type of interrupt is

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| called Hardw | are interrupt | | |
|---|----------------------------------|--|--|
| Softwa | are interrupt | | |
| Proces | sor exception | | |
| Logical | interrupts | | |
| Question No: 14 | (Marks: 1) - Please choose one | | |
| Which mathematical operation is dominant during the execution of SCAS instruction | | | |
| Divis | ion | | |
| Multi | plication | | |
| Addit | ion | | |
| Subtr | raction | | |
| Question No: 15 | (Marks: 1) - Please choose one | | |

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After the execution of REP instruction CX will be decremented then which of the following flags will be affected?

| CF | http://www.vustudents.net |
|------------------|--|
| OF | |
| DF | |
| No flags w | ill be affected |
| Question No: 16 | (Marks: 1) - Please choose one |
| is one | of the reasons due to which string instructions are used in 8088 |
| | |
| Efficie | ency and accuracy |
| Reduc | ction in code size and accuracy |
| Reduc | ction in code size and speed |
| Reduc | ction in code size and efficiency |
| Question No: 17 | (Marks: 1) |
| Write any two co | ntrol instructions. |

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| Question No: 18 | (Marks: 1) |
|----------------------|-----------------------------------|
| RET instruction take | e how many arguments |
| | |
| | |
| Question No: 19 | (Marks: 2) |
| | |
| Explain the fuction | of rotate right (ROR) instruction |
| | |
| Question No: 20 | (Marks: 2) |
| Describe the PUSH | function |
| | |
| Question No: 21 | (Marks: 3) |
| | |
| Write down the nan | nes of four segment registers? |
| | |
| | |
| | |
| Question No: 22 | (Marks: 3) |
| | |
| For what purpose "l | NT 4" is reserved? |

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| | Question No: 23 (N | larks: 5) | |
|--------------------|----------------------------|-----------|-----|
| | Given that [BX+0x0100] | BX=0x0100 | |
| | | Ds=0xFFF0 | |
| | Calculate the physical a | ddress | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| Question No: 1 (| (Marks: 1) - Please choos | se one | |
| | | | The |
| physical address o | f the stack is obtained by | | |
| 3 SS:SP combinati | on | | |
| 2 SS:SI (| combination | | |
| | | | |
| 42·22 ₪ | combination | | |
| 2 00.01 | | | |
| | | | |

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| 2 ES:BP combination | n | |
|---|--------------------------------------|---------|
| 2 ES:SP combination | n | |
| Question No: 2 (Marks: 1) | - Please choose one | After |
| the execution of instruction "R | RET " | — Arter |
| ☑ SP is incremented by 2 | | |
| 2 SP is incremented by 2 | | |
| | | |
| | | |
| | | |
| Question No: 3 (Marks: 1) | - Please choose one | |
| | | The |
| | gnated for one screen location holds | |
| Character color on t | the screen | |
| ☑ The dimensions of the dimension of t | the screen | |

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| © Character position on the screen | |
|---|--------------|
| ☐ Character color on the screen | |
| ☑ ASCII code of the character | |
| Question No: 4 (Marks: 1) - Please choose one | REP |
| will always | KLI |
| Decrement CX by 1 | |
| Increment CX by 1 | |
| Increment CX by 2 | |
| Decrement CX by 1 | |
| ☑ Decrement CX by 2 | |
| Question No: 5 (Marks: 1) - Please choose one | T h e |
| basic function of SCAS instruction is to | |

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② Compare

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Compare

| Index registers are used to store | |
|---|-----|
| 222222222222Address | |
| 2222222Both data and addresses | |
| Question No: 7 (Marks: 1) - Please choose one | |
| | The |
| bits of the work independently and individually | |
| 22222222222222222222222222222222222222 | |
| 22index register | |
| 222222222base register | |
| 2222222flags register | |
| 222222222accumulator | |
| | |
| Question No: 8 (Marks: 1) - Please choose one | |
| | То |
| convert any digit to its ASCII representation | |

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Subtract 0x30 from the digit

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| ☑ Add 0x61 in the digit |
|--|
| ☑ Subtract 0x61 from the digit |
| Question No: 9 (Marks: 1) - Please choose one |
| When a 32 bit number is divided by a 16 bit number, the quotient is of |
| ☑ 4 bits Question No: 10 (Marks: 1) - Please choose one |
| When a 16 bit number is divided by an 8 bit number, the quotient will be in |
| 2 AX |
| 2 AL |
| 2 AH |
| ☑ DX |
| Question No: 11 (Marks: 1) - Please choose one |
| Which mathematical operation is dominant during the execution of SCAS instruction Provision |

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| Question No: 12 (Marks: 1) - Please choose one | If AX |
|--|-------|
| contains decimal -2 and BX contains decimal 2 then after the execution of instructions: | II AA |
| CMP AX, BX | |
| JA label | |
| Zero flag will set | |
| 2 Jump will be taken | |
| ☑ Zero flag will set | |
| 2 ZF will contain value -4 | |
| ☑ Jump will not be taken | |
| Question No: 13 (Marks: 1) - Please choose one | The |
| execution of the instruction "mov word [ES: 160], 0x1230" will print a character "0" on the screen | |
| Second column of first row | |
| ☑ First column of second row | |
| Second column of second row | |
| ☑ First column of third row | |

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| Question No: 14 (Marks: 1) - Please choose one | |
|--|--------------|
| direction of the processing of a string is from higher addresses towards lower addresses the | If the en |
| | |
| ② DF is cleared | |
| | |
| ☑ DF is set | |
| Question No: 15 (Marks: 1) - Please choose one | |
| instruction ADC has Operand(s) | The |
| | |
| ② 0 | |
| ⊡ 1 | |
| ② 2 | |
| 23 | |

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| Question No: 16 (Marks: 1) - Please choose one |
|--|
| Which bit of the attributes byte represents the red component of background color? |
| 23 |
| |
| 2 4 |
| 2 5 |
| 2 6 |
| |
| Q=12 |
| Int 13-bios disk service "generally uses which register to return the error flag? |
| CF DL AH AL |
| |
| Q=13: |
| The first sector on the hard disk contains the |
| Hard disk size Partition table Data size |
| Sector size |
| |
| Q=14 |

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| | ting system organize data in the form of |
|---------|---|
| • | Folder Batch file File |
| • | None of above |
| | |
| | http://www.vustudents.net |
| | |
| | |
| Q=15 | |
| In 9 pi | n db 9 connector, which pin is assigned to TD(transmitted data) |
| • | |
| | |
| • | 1 2 |
| • | 3 |
| • | 4 |
| | |
| | |
| | |
| Q=16" | |
| | |
| Device | e derive can be divided intomajor categories. |
| • | 5 |
| | 4 |
| • | 9 |
| • | 3 2 |

- 1. BL contains 5 decimal then after right shift, BL will become
 - 3

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| 2.5510 | |
|--|--|
| 2. 8 * 16 font is stored in bytes. • 3 • 4 • 8 • 16 | |
| 3. In DOS input buffer , number of characters actually read on return is stored in First byte Second byte Third byte Fourth byte | |
| 4. IRQ 0 has priority Low High <u>Highest</u> Medium | |
| 5. Thread registration code initialize PCB and add to linked list so that will give it turn. Assembler Linker Scheduler Debugger | |
| 6. Traditional calling conventions are in number | |
| 1 2 3 4 | |
| 7. VESA VEB 2.0 is standard for High Resolution Mode Low Resolution Mode Very High Resolution Mode Medium Resolution Mode | |
| 8. To clear direction flag which instruction is used | |
| • Cld • Clrd | |

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- Cl df
- Clr df
- 9. In STOSW instruction, When DI is cleared, SI is
 - Incremented by 1
 - Incremented by 2
 - Decremented by 1
 - Decremented by 2
- 10. Interrupt that is used in debugging with help of trap flag is
 - INT 0
 - <u>INT 1</u>
 - INT 2
 - INT 3
- 11. INT for arithmetic overflow is
 - INT 1
 - INT 2
 - INT 3
 - INT 4
- 12. IRQ referred as
 - Eight Input signals
 - One Input signal
 - Eight Output signals
 - One output signal
- 13. IRQ for keyboard is _____1
- 14. IRQ for sound card is ______5
- 15. IRQ for floppy disk is ______6
- 16. IRQ with highest priority is
 - Keyboard IRQ
 - Timer IRQ
 - Sound Card
 - Floppy Disk
- 17. Pin for parallel port ground is
 - 10-18

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| • | 18-25 25-32 32-39 |
|------------------|--|
| 18. Th | ne physical address of Interrupt Descriptor Table (IDT) is stored in GDTR IDTR IVT IDTT |
| 19. Ex | recution of "RET 2" results in? |
| 20. C | Cregister is Count register Data register Index register Base register |
| 21. OI | JT instruction uses <mark>AX_</mark> as source register. |
| • | DB-9 connector the Data Set ready pin is at 5 6 7 8 |
| 23. If t | two devices uses same IRQ then there is IRQ collision IRQ conflict IRQ drop |
| 24. VE • • | ESA organizes 16 bit color for every pixel in ratio 5:5:5 5:6:5 6:5:6 5:6:7 |
| 25. Di | vision by zero is done by which interrupt. Interrupt 0. |
| | |

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| Question No: 1 (Marks: 1) - Please choose one | |
|--|-------|
| the execution of SAR instruction | After |
| The msb is replaced by a 0 | |
| ► The msb is replaced by 1 | |
| ► The msb retains its original value | |
| ► The msb is replaced by the value of CF | |
| Question No: 2 (Marks: 1) - Please choose one | |
| will pop the offset in the | RETF |
| ▶ BP | |
| <u>▶</u> IP | |
| ► SP | |
| ► SI | |
| Question No: 3 (Marks: 1) - Please choose one | |
| routing that executes in response to an INT instruction, is called | The |
| routine that executes in response to an INT instruction is called | |

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| ▶ ISR | | |
|---------------------|----------------------------------|-------|
| ► IRS | | |
| ► ISP | http://www.vustudents.net | |
| ► IRT | | |
| Question No: 4 | (Marks: 1) - Please choose one | The |
| first instruction (| of "COM" file must be at offset: | The |
| ► 0x0010 | | |
| ► 0x0100 | | |
| ► 0x1000 | | |
| ► 0x0000 | | |
| Question No: 5 | (Marks: 1) - Please choose one | "Far" |
| jump is not posit | ion relative but is | — гаі |
| ► memory | dependent | |
| ► Absolute | | |
| ► tempora | ry | |

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▶ indirect

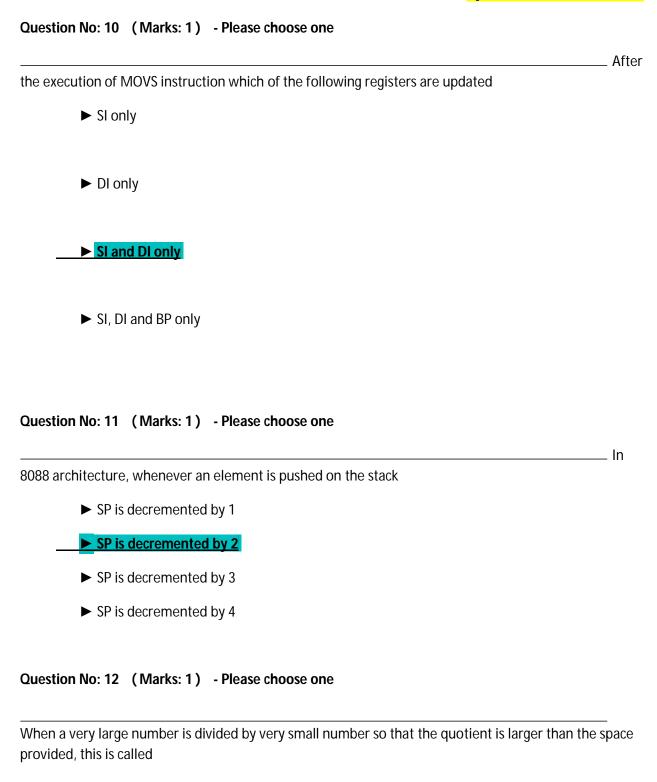
| | Only |
|--|-------|
| instructions allow moving data from memory to memory. | |
| | |
| <u>▶ string</u> | |
| ► word | |
| ► indirect | |
| ► stack | |
| | |
| | |
| Question No: 7 (Marks: 1) - Please choose one | |
| | After |
| | After |
| Question No: 7 (Marks: 1) - Please choose one the execution of instruction "RET 2" > SP is incremented by 2 | After |
| | After |
| the execution of instruction "RET 2" SP is incremented by 2 | After |
| the execution of instruction "RET 2" | After |
| the execution of instruction "RET 2" SP is incremented by 2 SP is decremented by 2 | After |
| the execution of instruction "RET 2" SP is incremented by 2 | After |
| the execution of instruction "RET 2" SP is incremented by 2 SP is decremented by 2 | After |

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| Question No: 8 (Marks: 1) - Please choose one | |
|--|-----|
| instruction has | DIV |
| Two forms | |
| ► Three forms | |
| ► Four forms | |
| ► Five forms | |
| Question No: 9 (Marks: 1) - Please choose one | |
| When the operand of DIV instruction is of 16 bits then implied dividend will be of | |
| ► 8 bits | |
| ► 16 bits | |
| ▶ 32 bits | |
| ► 64 hits | |

CS401-Computer Architecture & Assembly Language Programming

By:-Talal Hasnat Awan



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| ► Divide logical error | |
|--|------------|
| Divide overflow error | |
| ► Divide syntax error | |
| ► An illegal instruction | |
| Overtion No. 12 (Marks 1) Disease the sea are | |
| Question No: 13 (Marks: 1) - Please choose one | ₋ In |
| the word designated for one screen location, the higher address contains | - 111 |
| ► The character code | |
| ► The attribute byte | |
| ► The parameters | |
| ► The dimensions | |
| Question No: 14 (Marks: 1) - Please choose one | |
| Which of the following options contain the set of instructions to open a window to the video men | - nory? |
| ► mov AX, 0xb008 | |
| mov ES, AX | |
| <u>▶ mov AX, 0xb800</u> | |

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| mov ES, AX | |
|--|------|
| ► mov AX, 0x8b00 | |
| ES, AX | |
| ► mov AX, 0x800b | |
| mov ES, AX | le o |
| Question No: 15 (Marks: 1) - Please choose one | |
| video memory, each screen location corresponds to | In a |
| ► One byte | |
| Two bytes | |
| ► Four bytes | |
| ► Eight bytes | |
| Question No: 16 (Marks: 1) - Please choose one execution of the instruction "mov word [ES: 0], 0x0741" will print character "A" on screen, background color of the screen will be | The |
| Black | |
| ► White | |
| ► Red | |

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► Blue

Question No: 1 ___(Marks: 1) - Please choose one

Which of the following is not true about registers?

- 1. Their operation is very much like memory
- 2. Intermediate results may also be stored in registers.
- 3. They are also called scratch pad ram
- 4. None of given options.

Question No: 2 ___(Marks: 1) - Please choose one

move [bp], all moves the one byte content of the AL register to the address contained in BP register in the current

- 1. Stack segment
- 2. Code segment
- 3. Data segment
- 4. Extra segment

Question No: 3 (Marks: 1) - Please choose one

In a rotate through carry right (RCR) instruction applied on a 16 bit word Effectively there is

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| 1 | 1 | 16 | hit | -C I | rot | tati | ior | ١ |
|---|---|----|-----|------|-----|------|-----|---|
| | | טו | υII | SI | ΙUΙ | lal | UI | ı |

- 2. 1 bit rotation
- 3. 17 bits rotation
- 4. 8 bits rotation

Question No: 4__ (Marks: 1) - Please

choose one The 8088 stack works on

- 1. Word sized elements
- 2. Byte sized elements
- 3. Double sized element
- 4. Nible sized element

Question No: 5 (Marks: 1) - Please

choose one

An 8 x 16 font is stored in.....Bytes

- 1. 2
- 2. 4
- 3. 8
- 4. 16

Question No: 6 (Marks: 1) - Please

INT 10 is used for.....services.

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| 3. BIOS video4. DOS video |
|---|
| Question No: 7 (Marks: 1) - Please choose one |
| Priority of IRQ 0 interrupt is |
| medium high highest low |
| Question No: 8 (Marks: 1) - Please choose one |
| Threads can have function calls, parameters andvariables. |
| 1. global 2. local 3. legal 4. illegal |
| Question No: 9 (Marks: 1) - Please choose |
| one How many prevalent calling conventions doexist |
| |
| 1. 1 2. 2 3. 3 |
| 3. 3 4. 4 |
| |

Question No: 10 (Marks: 1) - Please choose

RAM
 Disk

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| , |
|---|
| one In 9pin DB 9 DSR is assigned on pin number |
| 1. 4 2. 5 3. 6 4. 7 |
| Question No: 11 |
| (Marks: 1) - Please |
| choose one In 9pin DB 9 CTS is assigned on pin |
| number |
| 1. 6 2. 7 3. 8 4. 9 |
| Question No: 12_ (Marks: 1) - Please choose one |
| In 9pin DB 9 CD is assigned on pin number |
| 1. 1 2. 2 3. 3 4. 4 |
| Question No: 13 (Marks: 1) - Please choose one |

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In 9pin DB 9 RD is assigned on pin number

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Question No: 14 __ (Marks: 1) - Please choose one

in device attribute word which of the following bit decides whether it is a cha rater

- 1. device or a block device
- 2. Bit 12 Bit 13
- 3. Bit 14
- 4. Bit 15

Question No: 15_ (Marks: 1) - Please choose one

Video servioces are classified into _____broad categories

- 2
- 3
- 4
- 5

Question No: 16 (Marks: 1) - Please choose

One

In STOSB instruction, when DF is clear, SI

Is.....(wrong question) The implied source will always be in AL or AX. If DF is clear, DI will be

incremented by one or two depending of whether STOSB or STOSW is used.

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If DF is set DI will be decremented by one or two depending of whether STOSB or STOSW is used.......if we put DI here instead of SI again its confusing

- 1. Incremented by 1
- 2. Incremented by 2
- Decremented by 1
- 4. Decremented by 2

Question No: 17 (Marks: 1) - Please choose one The

Process of sending signals back and forth is called

- 1. Activity
- 2. Hand-shaking
- 3. Interruption
- 4. Time clicking

Question No: 18 (Marks: 1) - Please choose one

which of the following is a special type of interrupt that returns to the same instruction instead of the next instruction

- 1. Divide overflow interrupt
- 2. Debug interrupt
- 3. Arithmetic overflow interrupt
- 4. Change of sign interrupt

Question No: 19 ___(Marks: 1) - Please choose one

Which of the following IRQs is derived by a timer device?

1. IRQ 0

2. IRQ 1

3. IRQ 2

| _ | _ | | | | | | | |
|-------|-----|-----|---|----|-----|----|----|---|
| By :- | l a | lal | Н | as | nat | ΞA | wa | n |

4. IRQ 3

Question No: 20 __ (Marks: 1) - Please choose one

Which of the following interrupts is used for Arithmetic overflow

- 1. INT 1
- 2. INT 2
- 3. INT 3
- 4. INT 4

Question No: 21 __ (Marks: 1) - Please choose one

Which of the following IRQs is connected to serial port COM 2?

- 1. IRQ 0
- 2. IRQ 1
- 3. IRQ 24. IRQ 3

Question No: 22 __ (Marks: 1) - Please

choose one

An End of Interrupt (EOI) signal is sent by

- 1. Handler
- 2. Processor
- 3. IRQ

Question No: 23 __ (Marks: 1) - Please choose one

The source registers in OUT is

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- 2. BL or BX
- 3. CL or CX
- 4. DL or DX

Question No: 24 (Marks: 1) - Please choose one

In programmable interrupt controller which of the following ports is used for selectively enabling or disabling interrupts

- 1. 19
- 2. 20
- 3. 21
- 4. 22

Question No: 25 (Marks: 1) - Please choose one

The number of pins in a parallel port connector

are?



- 2 30
- 3. 35

Question No: 26 (Marks: 1) - Please choose one

Which of the following pins of a parallel port connector are grounded?

1. 10-18

2. 18-25

3. 25-32

4. 32-39

Question No: 27 __ (Marks: 1) - Please choose one

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Suppose a decimal number 35 when its binary is shifted to write two places the new number will become

- 1. 35
- 2. 70
- 3. 140
- 4. 17

Question No: 28 __ (Marks: 1) - Please choose one

A 32bit address register can access uptoof memory so memory access has increased a lot.

- 1. 2GB
- 2. 4GB
- 3. 6GB
- 4. 8GB

Question No: 29 __ (Marks: 1) - Please choose one

In NASM an imported symbol is declared with thewhile and exported symbol is declared with the

- 1. Global directive, External directive
- 2. External directive, Global directive
- 3. Home Directive, Foreign Directive
- 4. Foreign Directive, Home Directive

Question No: 30 (Marks: 1) - Please choose

one Single step interrupt is

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- 1. Hardware interrupt
- 2. Like divide by zero interrupt
- 3. Like divide by 1 interrupt
- 4. Software interrupt

Question No: 31 __ (Marks: 1)

Which services are gained bi INT 0x16

Solution:

Hardware interrupt

Like divide by zero interrupt

Like divide by 1 interrupt

Software interrupt

Question No: 32 (Marks: 1

Give the name of any one VESA servic

- Hardware interrupt
- Like divide by zero interrupt
- Like divide by 1 interrupt
- Software interrupt

Question No: 33 (Marks: 2)

INT 14 - SERIAL - READ CHARACTER FROM PORT

By using above port what do AH,AL and DX shows here?

Hardware interrupt

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- Like divide by zero interrupt
- Like divide by 1 interrupt
- Software interrupt

Question No: 34 (Marks: 2)

What do these instructions do? write your answer in single line.

mov cx, 0xffff

loop\$

- Hardware interrupt
- Like divide by zero interrupt
- Like divide by 1 interrupt
- Software interrupt

Question No: 35 (Marks: 3) Define the protected mode

Solution:

- Hardware interrupt
- Like divide by zero interrupt
- Like divide by 1 interrupt
- Software interrupt

Question No: 36 (Marks: 3)

Write a program in assembly language to disable keyboard interrupt using PIC

mask register

Hint: Only five instructions are needed

Solution:

- Hardware interrupt
- Like divide by zero interrupt
- Like divide by 1 interrupt
- Software interrupt

Question No: 37 (Marks: 3)

Read the following passage carefully and fill the blanks with proper words.

Note: Don't rewrite the passage just write the words in same order.

"BIOS sees the disks as a combination of sectors, tracks, and....., as a raw storage device without concern to whether it is reading a file or directory.

| | _ | _ | | | | | | | |
|----|------|----|----|---|------|-----|---|----|---|
| Βy | / :- | la | al | Н | lasi | nat | A | wa | n |

| medi store | provides the simplest and most powerful interface to the storage medium. However this raw storage is meaningless to the user who needs to store his files and organize them into | | | | | | |
|---|--|-------------------|--|--|--|--|--|
| • | | | | | | | |
| _ | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| Ques | stion No: 1 (Marks: 1) | | | | | | |
| - Plea | ase choose one | | | | | | |
| Sun S | SPARC Processor has a fixed | instruction size. | | | | | |
| 2. 3. | . 16bit 2. 32bit 3. 64bit 4. 20bit | | | | | | |
| Ques | stion No: 2 (Marks: 1) | | | | | | |
| - Plea | ase choose one | | | | | | |
| When the subprogram finishes, the retrieves the return address from the stack and transfers control to that location. | | | | | | | |
| 2. | . RET instruction 2. CALL instruction 3. POP instruction | | | | | | |

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4. Jump instruction

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| Question No: 3 (Marks: 1) |
|---|
| - Please choose one |
| A 32 bit address register can access upto of memory. |
| 1 GB 6 GB 4 GB 2 GB |
| Question No: 4 (Marks: 1) |
| - Please choose one |
| The value of a segment register when the processor is running under protected mode is called |
| segment descriptor segment selector global descriptor table protected register |
| Question No: 5 (Marks: 1) |

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| - Please choose one | |
|--|--------------|
| FS and GS are two in protected n | node. |
| segment registers segment selectors stack pointers register pointers | |
| Question No: 6 (Marks: 1) | |
| - Please choose one | |
| IRQ 0 interrupt have priority | |
| low medium highest lowest | |
| Question No: 7 (Marks: 1) | |
| - Please choose one | |
| IDT stands for | |
| interrupt descriptor table individual descriptor table inline data table interrupt descriptor table | |
| Question No: 8 (Marks: 1) | |
| - Please choose one | |
| Every bit of line status in serial port conveys | information. |

1. different

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| 3. partial4. full | http://www.vustudents.net |
|---|--|
| Question No: | 9 (Marks: 1) |
| - Please choos | e one |
| There are total | bytes in a standard floppy disk. |
| 1. 1444k 2. 1440k 3. 1280k 4. 2480k | |
| Question No: | 10 (Marks: 1) |
| - Please choos | e one |
| An 8x16 font is | stored in bytes. |
| 816420 | |
| 3FF while | also accessible via |
| Other register of available interrupt. | of our interest include 3F9 whose <u>Bit 0</u> must be set to enable received data upt and <u>Bit 1</u> must be set to enable transmitter holding register empty |

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(Transmitter, COM 1, I/O ports, COM2. bit 0, Buffer, 3FA)

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| Overtine #4 |
|---|
| Question # 1 There are three busses to communicate the processor and memory named as |
| Question # 2 The address bus is unidirectional and address always travels from processor to memory. 1): TRUE 2): FALSE 3): 4): Correct Option: 1 From: Lecture 1 |
| Question # 3 Data bus is bidirectional because 1): To way 2): Data moves from both, processor to memory and memory to processor, 3): Data moves from both, processor to memory and memory to data Bus, 4): None of the Given Correct Option: 3 From: Lecture 1 |
| Question # 4 Control bus 1): is Not Important. 2): is Important. 3): bidirectional. 4): unidirectional. Correct Option: 3 From: Lecture 1 |
| Question # 5 A memory cell is an n-bit location to store data, normallyalso called a byte 1): 4-bit 2): 8-bit 3): 6-bit 4): 80-bit |

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| Correct Option : 2 From : Lecture 1 |
|--|
| Question # 6 The number of bits in a cell is called the cell width define the memory completely. 1): Cell width and number of cells, 2): cell number and width of the cells, 3): width 4): Height Correct Option: 1 From: Lecture 1 |
| Question # 7 for memory we define two dimensions. The first dimension defines how manybits are there in a single memory cell. 1): parallel 2): Vertical 3): long 4): short Correct Option: 1 From: Lecture 1 |
| Question # 8 operation requires the same size of data bus and memory cell width. 1): Normal 2): Best and simplest 3): first 4): None of the Given Correct Option: 2 From: Lecture 1 |
| Question # 9 Control bus is only the mechanism. The responsibility of sending the appropriate signals on the control bus to the memory is of the 1): Data Bus 2): processor 3): Address Bus 4): None of the Given Correct Option: 2 From: Lecture 1 |
| Question # 10 In "total: dw 0 " Opcode total is a 1): Literal 2): Variable |

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| 3) : Label 4) : Starting point Correct Option : 3 From : Lecture 10 |
|---|
| Question # 11 0 1 1 0 1 0 0 0 C is a example of 1) : ShI 2) : sar 3) : Shr 4) : SaI Correct Option : 3 From : Lecture 10 |
| Question # 12 C (1 1 0 1 0 0 0 (0 is a example of 1) : ShI 2) : sar 3) : Shr 4) : Sal Correct Option : 1 From : Lecture 10 |
| Question # 13 ADC has operands. 1): two 2): three 3): Five 4): Zero Correct Option: 2 From: Lecture 10 |
| Question # 14 The basic purpose of a computer is to perform operations, and operations need |
| 1): order 2): nothing 3): operands 4): bit Correct Option: 3 From: Lecture 2 |
| Question # 15 Registers are like a scratch pad ram inside the processor and their operation is very much like normal 1): Number |

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| 2) : opreations 3) : memory cells 4) : None of the Given Correct Option : 3 From : Lecture 2 |
|---|
| Question # 16 There is a central register in every processor called the and The word size of processor is defined by the width of its 1): accumulator,accumulator 2): data bus,accumulator 3): accumulator, Address Bus 4): accumulator,memory Correct Option: 1 From: Lecture 2 |
| Question # 17does not hold data but holds the address of data 1): Pointer, Segment, or Base Register 2): Pointer, Index, or Base Register 3): General Registers 4): Instruction Pointer Correct Option: 2 From: Lecture 2 |
| Question # 18 "The program counter holds the address of the next instruction to be" 1): executed. 2): called 3): deleted 4): copy Correct Option: 1 From: Lecture 2 |
| Question # 19 There are types of "instruction groups" 1): 4 2): 5 3): 3 4): 2 Correct Option: 1 From: Lecture 2 |
| Question # 20 These instructions are used to move data from one place to another. |

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1): TRUE

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| 2): FALSE 3): 4): Correct Option: 1 From: Lecture 2 |
|--|
| Question # 21 "mov" instruction is related to the *****. 1) : Arithmetic and Logic Instructions 2) : Data Movement Instructions 3) : Program Control Instructions 4) : Special Instructions Correct Option : 2 From : Lecture 2 |
| Question # 22allow changing specific processor behaviors and are used to play with it. 1): Special Instructions 2): Data Movement Instructions 3): Program Control Instructions 4): Arithmetic and Logic Instructions Correct Option: 1 From: Lecture 2 |
| Question # 23 8088 is a 16bit processor with its accumulator and all registers of 1): 32 bits 2): 6 bits 3): 16 bits 4): 64 bits Correct Option: 3 From: Lecture 2 |
| Question # 24 The of a processor means the organization and functionalities of the registers it contains and the instructions that are valid on the processor. 1): Manufactures 2): architecture 3): Deal 4): None of the Given Correct Option: 2 From: Lecture 2 |
| Question # 25 Intel IAPX88 Architecture is 1): More then 25 old |

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| 2): New 3): Not Good 4): None of the Given Correct Option: 1 From: Lecture 2 |
|---|
| Question # 26 The iAPX88 architecture consists ofregisters. 1): 13 2): 12 3): 9 4): 14 Correct Option: 4 From: Lecture 3 |
| Question # 27 General Registers are 1): AX, BX, CX, and DX 2): XA, BX, CX, and DX 3): SS,SI and DI 4): 3 Correct Option: 1 From: Lecture 3 |
| Question # 28 AX means we are referring to the extended 16bit "A" register. Its upper and lower byte are separately accessible as 1): AH and AL 2): A Lower and A Upper 3): AL, AU 4): AX Correct Option: 1 From: Lecture 3 |
| Question # 29 AX is General purpose Register where A stands for 1): Acadmic 2): Ado 3): Architecture 4): Accumulator Correct Option: 4 From: Lecture 3 |
| Question # 30 The B of BX stands forbecause of its role in memory addressing. 1): Busy |

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| 2): Base3): Better4): None of the GivenCorrect Option: 2 From: Lect | http://www.vustudents.net |
|---|---|
| Question # 31 | nation as it acts as the destination in |
| Question # 32 The C of CX stands for Count count in the 1): DI register 2): BX register 3): CX register 4): DX register Correct Option: 3 From: Lect | er as there are certain instructions that work with an automatic ture 3 |
| Question # 33are the index regis in memory access. 1): SI and SS 2): PI and DI 3): SI and IP 4): SI and DI Correct Option: 4 From: Lect | sters of the Intel architecture which hold address of data and used |
| Question # 34 In Intel IAPX88 architecture next instruction to be executed 1): AX 2): PI 3): IP 4): SI Correct Option: 3 From: Lect Question # 35 | |
| Question # 35 | |

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| SP is a memory pointer and is used indirectly by a set of 1): instructions 2): Pointers 3): Indexes 4): Variables Correct Option: 1 From: Lecture 3 |
|--|
| Question # 36is also a memory pointer containing the address in a special area of memory called the stack. 1): SP 2): BP 3): PB 4): AC Correct Option: 2 From: Lecture 3 |
| Question # 37is bit wise significant and accordingly each bit is named separately. 1): AX 2): FS 3): IP 4): Flags Register Correct Option: 4 From: Lecture 3 |
| Question # 38 When two 16bit numbers are added the answer can be 17 bits long, this extra bit that won't fit in the target register is placed in thewhere it can be used and tested 1): carry flag 2): Parity Flag 3): Auxiliary Carry 4): Zero Flag Correct Option: 1 From: Lecture 3 |
| Question # 39 Program is an ordered set of instructions for the processor. 1): TRUE 2): FALSE 3): 4): Correct Option: 1 From: Lecture 3 |

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| Question # 40 |
|--|
| For Intel Architecture "operation destination, source" is way of writing things. |
| 1): TRUE |
| 2): FALSE |
| 3): |
| 4): |
| Correct Option: 1 From: Lecture 3 |
| Question # 41 |
| Operation code " add ax, bx " |
| 1) : Add the bx to ax and change the bx |
| 2): Add the ax to bx and change the ax |
| 3): Add the bx to ax and change the ax |
| 4) : Add the bx to ax and change nothing |
| Correct Option: 3 From: Lecture 3 |
| Question # 42 |
| The maximum memory iAPX88 can access is |
| 1) : 1MB |
| 2): 2MB |
| 3) : 3MB |
| 4) : 128MB |
| Correct Option : 1 From : Lecture 4 |
| Question # 43 |
| The maximum memory iAPX88 can access is 1MB which can be accessed with |
| 1): 18 bits |
| 2): 20 bits |
| 3): 16 bits |
| 4): 2 bits |
| Correct Option : 2 From : Lecture 4 |
| Question # 44 |
| address of 1DED0 where the opcode B80500 is placed. |
| 1) : physical memory |
| 2) : memory |
| 3) : efective |
| 4): None of the Given |
| Correct Option: 1 From: Lecture 4 |

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| Question # 45 16 bit of Segment and Offset Addresses can be converted to 20bit Address i.e |
|--|
| Segment Address with lower four bits zero + Offset Address with four bits zero = 20bit Physical Address 1): Middle 2): lower 3): Top 4): upper |
| Correct Option: 4 From: Lecture 4 |
| Question # 46 When adding two 20bit Addresses a carry if generated is dropped without being stored anywhere and the phenomenon is called address 1): wraparound 2): mode 3): ping 4): error Correct Option: 1 From: Lecture 4 |
| Question # 47 segments can only be defined a 16byte boundaries called boundaries. 1): segment 2): paragraph 3): Cell 4): RAM Correct Option: 1 From: Lecture 4 |
| Question # 48 in a Program CS, DS, SS, and ES all had the same value in them. This is called |
| 1): equel memory 2): overlapping segments 3): segments hidding 4): overlapping SI Correct Option: 2 From: Lecture 4 |
| Question # 49 "db num1" size of the memory is 1) : 1byte 2) : 4bit 3) : 16bit |

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| 4): 2byte | | |
|---|--|--|
| Correct Option : 1 From : Lecture 5 | | |
| Question # 50 | | |
| " 1[org 0x0100] | | |
| 2mov ax, [num1]; load first number in ax | | |
| 3mov bx, [num2]; load second number in bx | | |
| 4add ax, bx | | |
| 5int 0x21 | | |
| 6 | | |
| 7num1: dw 5 | | |
| 8num2: dw 10 | | |
| | | |
| Comments for the 4 are : | | |
| 1): No comments Will be | | |
| 2) : ; accumulate sum in add | | |
| 3) : ; accumulate sum in ax | | |
| 4) : ; accumulate sum in Bx | | |
| Correct Option : 3 From : Lecture 5 | | |
| | | |
| Question # 51 | | |
| In "mov ax, bx" is Addressing Modes. | | |
| 1) : Immediate | | |
| 2) : Indirect | | |
| 3): Direct | | |
| 4) : Register | | |
| Correct Option : 4 From : Lecture 5 | | |
| Question # 52 | | |
| In "mov ax, [bx] " is Addressing Modes | | |
| 1): Based Register Indirect | | |
| 2) : Indirect | | |
| 3) : Base Indirect | | |
| 4) : Immediate | | |
| Correct Option : 1 From : Lecture 5 | | |
| · | | |
| ()uestion # 53 | | |
| Question # 53 In "mov ax 5" is Addressing Modes | | |
| In "mov ax, 5" is Addressing Modes 1): Immediate | | |

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| Question # 58 | |
|--|-------------------|
| For example | |
| BX=0100 | |
| DS=FFF0 | |
| And Opcode are; | |
| move [bx+0x0100], Ax | |
| now what is the physical memory add | dress; |
| 1) : 0020 | |
| 2) : 0x0100 | |
| 3) : 0x10100 | |
| 4) : 0x100100 | |
| Correct Option: 2 From: Lecture 7 | |
| Question # 59 | |
| In " mov [1234], al " is | Addressing Modes. |
| 1) : Immediate | |
| 2) : Indirect | |
| 3) : Direct | |
| 4) : Register | |
| Correct Option : 3 From : Lecture 8 | |
| Question # 60 | |
| In " mov [SI], AX " is | Addressing Modes. |
| 1) : Basef Register Indirect | |
| 2) : Indirect | |
| 3) : Indexed Register Indirect | |
| 4) : Immediate | |
| Correct Option : 3 From : Lecture 8 | |
| Question # 61 | |
| In " mov ax, [bx - Si] " is | ADDRESSING |
| 1) : Basef Register Indirect | _ |
| 2) : Indirect | |
| 3) : Direct | |
| 4) : illegal | |
| Correct Option: 4 From: Lecture 8 | |
| Question # 62 | |
| In " mov ax, [BL] " there is error i.e. $_$ | |
| 1): Address must be 16bit | |

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| 2) : Address must be 8bit 3) : Address must be 4bit 4) : 8 bit to 16 bit move illegal Correct Option : 4 From : Lecture 8 |
|---|
| Question # 63 In "mov ax, [SI+DI]" there is error i.e 1): Two indexes can't use as Memory Address 2): index can't use as Memory Address 3): I don't Know 4): None of the Given Correct Option: 1 From: Lecture 8 |
| Question # 64 In JNE and JNZ there is difference for only; 1): Programmer or Logic 2): Assembler 3): Debugger 4): IAPX88 Correct Option: 1 From: Lecture 9 |
| Question # 65 JMP is Instruction that on executing take jump regardless of the state of all flags is called 1): Jump 2): Conditional jump 3): Unconditional jump 4): Stay Correct Option: 3 From: Lecture 9 |
| Question # 66 When result of the source subtraction from the destination is zero, zero flag is set i.e. ZF=1 its mean that; 1): DEST = SRC 2): DEST!= SRC 3): DEST < SRC 4): DEST > SRC Correct Option: 1 From: Lecture 9 |

Question #67

When an unsigned source is subtracted from an unsigned destination and the destination is

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| smaller, borrow is needed which sets the |
|--|
| 1) : carry flag i.e CF = 0 |
| 2) : carry flag i.e CF = 1 |
| 3) : Carry Flag + ZF=1 |
| 4) : None of the Given |
| Correct Option: 2 From: Lecture 9 |
| Question # 68 |
| In the case of unassigned source and destination when subtracting and in the result ZF =1 OR |
| CR=1 then |
| 1): DEST = SRC |
| 2) : DEST != SRC |
| 3): UDEST? USRC |
| 4): DEST > SRC |
| Correct Option: 3 From: Lecture 9 |
| Question # 69 |
| In the case of unassigned source and destination when subtracting and in the result $ZF = 0$ AND |
| CR=0 then |
| 1) : DEST = SRC |
| 2) : DEST != SRC |
| 3): UDEST < USRC |
| 4) : UDEST > USRC Correct Option : 4 From : Lecture 9 |
| Correct Option : 4 From : Lecture 9 |
| Question # 70 |
| In the case of unassigned source and destination when subtracting and in the result CR=0 then |
| 1) : DEST = SRC |
| 2) : DEST != SRC |
| 3): UDEST < USRC |
| 4): UDEST? USRC |
| Correct Option : 4 From : Lecture 9 |
| Question # 71 |
| This jump is taken if the last arithmetic operation produced a zero in its destination. After |
| a CMP it is taken if both operands were equal. |
| 1) : Jump if zero(JZ)/Jump if equal(JE) |
| 2) : Jump if equal(JE) |
| 3) : Jump if zero(JZ) |
| 4) : No Jump fot This |

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| Correct Option: 1 From: Lecture 9 |
|--|
| Question # 72This jump is taken after a CMP if the unsigned source is smaller than or equal to the unsigned destination. 1): JBE(Jump if not below or equal) |
| 2): JNA(Jump if not above)/JBE(Jump if not below or equal)3): JNA(Jump if not above)4): No Jump fot ThisCorrect Option: 2 From: Lecture 9 |
| Question # 1 Numbers of any size can be added using a proper combination of 1): ADD and ADC |
| 2) : ABD and ADC 3) : ADC and ADC 4) : None of the Given Correct Option : 1 From : Lecture 11 |
| Question # 2 Like addition with carry there is an instruction to subtract with borrows called 1): SwB 2): SBB 3): SBC 4): SBBC Correct Option: 2 From: Lecture 11 |
| Question # 3 if "and ax, bx" instruction is given, There are operations as a result 1): 16 AND 2): 17 AND 3): 32 AND 4): 8 AND Correct Option: 1 From: Lecture 12 |
| Question # 4can be used to check whether particular bits of a number are set or not. 1): AND 2): OR 3): XOR 4): NOT |
| Correct Option: 1 From: Lecture 12 |

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| Question # 5can also be used as a masking operation to invert selective bits. |
|--|
| 1): AND 2): OR 3): XOR 4): NOT Correct Option: 3 From: Lecture 12 |
| Question # 6 Masking Operations are Selective Bit 1): Clearing, XOR, Inversion and Testing 2): Clearing, Setting, Inversion and Testing 3): Clearing, XOR, AND and Testing 4): None of the Given Correct Option: 2 From: Lecture 12 |
| Question # 7 The instruction allows temporary diversion and therefore reusability of code. 1): CALL 2): RET 3): AND 4): XOR Correct Option: 1 From: Lecture 13 |
| Question # 8 CALL takes a label as and execution starts from that label, 1): argument 2): Lable 3): TXt 4): Register Correct Option: 1 From: Lecture 13 |
| Question # 9 When theinstruction is encountered and it takes execution back to the instruction following the CALL. 1): CALL 2): RET 3): AND 4): XOR Correct Option: 2 From: Lecture 13 |

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| Question # 10 Both the instructions are commonly used as a pair, however |
|---|
| technically they are independent in their operation. |
| 1): RET and ADC |
| 2): Cal and SSb |
| 3) : CALL and RET |
| 4) : ADC and SSB |
| Correct Option: 3 From: Lecture 13 |
| Question # 11 |
| The CALL mechanism breaks the thread of execution and does not change registers, except |
| 1) : SI |
| 2) : IP |
| 3) : DI |
| 4) : SP |
| Correct Option: 2 From: Lecture 13 |
| Question # 12 |
| Stack is a that behaves in a first in last out manner. |
| 1) : Program |
| 2) : data structure |
| 3): Heap |
| 4): None of the Given |
| Correct Option: 2 From: Lecture 14 |
| Question # 13 |
| If is not available, stack clearing by the callee is a complicated process. |
| 1): CALL |
| 2) : SBB |
| 3): RET n |
| 4): None of the Given |
| Correct Option: 3 From: Lecture 14 |
| Question # 14 |
| When the stack will eventually become full, SP will reach 0, and thereafter wraparound |
| producing unexpected results. This is called stack |
| 1): Overflow |
| 2): Leakage |
| 3): Error |

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| 4) : Pointer Correct Option : 1 From : Lecture 14 |
|---|
| Question # 15 The pop operation makes a copy from the top of the stack into its 1): Register 2): operand 3): RET n 4): Pointer Correct Option: 2 From: Lecture 14 |
| Question # 16decrements SP (the stack pointer) by two and then transfers a word from the source operand to the top of stack 1): PUSH 2): POP 3): CALL 4): RET Correct Option: 1 From: Lecture 14 |
| Question # 17 POP transfers the word at the current top of stack (pointed to by SP) to the destination operand and then SP by two to point to the new top of stack. 1): increments 2): dcrements 3): ++ 4): Correct Option: 1 From: Lecture 14 |
| Question # 18 The trick is to use theandoperations and save the callers' value on the stack and recover it from there on return. 1): POP, ADC 2): CALL, RET 3): CALL, RET n 4): PUSH, POP Correct Option: 4 From: Lecture 14 |
| Question # 19 To access the arguments from the stack, the immediate idea that strikes is to them off the stack |

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| 1): PUSH 2): POP 3): CALL 4): Rrgister Correct Option: 2 From: Lecture 15 |
|---|
| Question # 20 push bp we are 1) : sending bp copy to stack 2) : making bp copy from stack 3) : pushing bp on the stack 4) : doing nothing Correct Option : 3 From : Lecture 15 |
| Question # 21 Local Variables means variables that are used within the |
| Question # 22 Standard ASCII has 128 characters with assigned numbers from 1): 1to 129 2): 0 to 127 3): 0 to 128 4): None of the Given Correct Option: 2 From: Lecture 16 |
| Question # 23 When is sent to the VGA card, it will turn pixels on and off in such a way that a visual representation of 'A' appears on the screen. 1): 0x60 2): 0x90 3): 0x30 4): 0x40 Correct Option: 4 From: Lecture 16 |
| Question # 24 |

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```
Which bit is refer to the Blinking of foreground character
1):6
2):7
3):5
4):3
Correct Option: 2 From: Lecture 16
Question #25
Which bit is refer to the Intensity component of foreground color
1):4
2):5
3):3
4):7
Correct Option: 3 From: Lecture 16
Question #26
Which bit is refer to the Green component of background color
1):1
2):5
3):3
4):7
Correct Option: 2 From: Lecture 16
Question #27
Which bit is refer to the Green component of foreground color
1):1
2):5
3):3
4):7
Correct Option: 1 From: Lecture 16
Question #28
String can be indicate bye given
1): db 0x61, 0x62, 0x63
2): db 'a', 'b', 'c'
3): db 'abc'
4): All of the above
Correct Option: 4 From: Lecture 16
Question #29
The first form divides a 32bit number in DX:AX by its 16bit operand and stores the
```

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| quoti | ent in AX |
|-----------------------|---|
| 1) : 16bit | |
| 2): 17bit | |
| 3): 32bit | http://www.vustudents.net |
| 4): 64bit | |
| Correct Option : 1 F | rom : Lecture 17 |
| Question # 30 | |
| The (| (division) used in the process is integer division and not floating point |
| division. | |
| 1): DIV instruction | |
| 2) : ADC instruction | |
| 3): SSB instruction | |
| 4) : DIVI instruction | |
| Correct Option : 1 F | rom : Lecture 17 |
| Question # 31 | |
| (m | nultiply) performs an unsigned multiplication of the source operand and the |
| accumulator. | |
| 1) : Multi | |
| 2) : DIV | |
| 3) : MUL | |
| 4) : Move | |
| Correct Option: 3 F | rom : Lecture 18 |
| Question # 32 | |
| | n on the screen can be calculated with the following formulae. |
| 1): location = (hypo | os * 80 + SP) * 3 |
| 2): location = (hypo | os * 80 + slocation) * 2 |
| 3) : location = (hy | pos * 80 + epos) * 2 |
| 4): None of the Giv | en |
| Correct Option : 3 F | rom : Lecture 18 |
| Question # 33 | |
| To play with string t | here are 5 instructions that are |
| 1): STOS, LODS, (| CMPS, SCAS, and MOVS |
| 2): MUL, DIV, ADD | , ADC and MOVE |
| 3): SSB, ADD, CMF | PS, ADC, and MOVS |
| 4): None of the Giv | en |
| Correct Option: 1 F | rom · Lecture 18 |

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| Question # 34 |
|---|
| transfers a byte or word from register AL or AX to the string element addressed by |
| ES:DI and updates DI to point to the next location. |
| 1): LODS |
| 2): STOS |
| 3): SCAS |
| 4) : MOVE |
| Correct Option : 2 From : Lecture 18 |
| Question # 35 |
| transfers a byte or word from the source location DS:SI to AL or AX and updates |
| SI to point to the next location. |
| 1): LODS |
| 2): STOS |
| 3): SCAS |
| 4) : MOVE |
| Correct Option: 1 From: Lecture 18 |
| Question # 36 |
| compares a source byte or word in register AL or AX with the destination string element |
| addressed by ES: DI and updates the flags. |
| 1): LODS |
| 2): STOS |
| 3): SCAS |
| 4) : MOVE |
| Correct Option: 3 From: Lecture 18 |
| Question # 37 |
| repeat the following string instruction while the zero flag is set and REPNE or |
| REPNZ repeat the following instruction while the zero flag is not set. |
| 1): REP or REPZ |
| 2) : REPE or REPZ |
| 3): REPE or RPZ |
| 4): RPE or REPZ |
| Correct Option : 2 From : Lecture 18 |
| Question # 38 |
| LES loads |
| 1): ES |
| 2) : DS |
| 3): PS |

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| 4) : LS Correct Option : 1 From : Lecture 20 |
|--|
| Question # 39 LDS loads 1): ES 2): DS 3): PS 4): LS Correct Option: 2 From: Lecture 20 |
| Question # 40 REP allows the instruction to be repeated times allowing blocks of memory to be copied. 1): DX 2): CX 3): BX 4): AX Correct Option: 2 From: Lecture 20 |
| Question # 41pops IP, then CS, and then FLAGS. 1): Ret n 2): REZA 3): REPE 4): IRET Correct Option: 4 From: Lecture 21 |
| Question # 42, Trap, Single step Interrupt 1): INT 0 2): INT 1 3): INT 3 4): INT 0 Correct Option: 2 From: Lecture 21 |
| Question # 43INT 2,NMI-Non Maskable Interrupt (option is not given) 1): INT 0 2): INT 1 3): INT 3 |

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| 4): INT 0 Correct Option: From: Lecture 21 |
|--|
| Question # 44 To hook an interrupt we change the corresponding to that interrupt. 1): SX 2): vector 3): AX 4): BX |
| Correct Option: 2 From: Lecture 22 |
| |
| |
| |
| |
| Question # 1 There are three busses to communicate the processor and memory named as |
| : address bus.,data bus and data bus. : addressing bus.,data bus and data bus. : address bus.,datamove bus and data bus. : address bus.,data bus and control bus Correct Option : 4 From : Lecture 1 |
| Question # 2 The address bus is unidirectional and address always travels from processor to memory. 1): TRUE |

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2): FALSE

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| Correct Option : 1 From : Lecture 1 |
|---|
| Question # 3 Data bus is bidirectional because 1): To way 2): Data moves from both, processor to memory and memory to processor; 3): Data moves from both, processor to memory and memory to data Bus, 4): None of the Given Correct Option: 2 From: Lecture 1 |
| Question # 4 Control bus 1): is Not Important. 2): is Important. 3): bidirectional. 4): unidirectional. Correct Option: 3 From: Lecture 1 |
| Question # 5 A memory cell is an n-bit location to store data, normallyalso called a byte 1): 4-bit 2): 8-bit 3): 6-bit 4): 80-bit Correct Option: 2 From: Lecture 1 |
| Question # 6 The number of bits in a cell is called the cell width define the memory completely. 1): Cell width and number of cells, 2): cell number and width of the cells, 3): width 4): Height Correct Option: 1 From: Lecture 1 |
| Question # 7 for memory we define two dimensions. The first dimension defines how manybits are there in a single memory cell. 1): parallel |

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| 2): Vertical 3): long 4): short Correct Option: 1 From: Lecture 1 |
|---|
| Question # 8 operation requires the same size of data bus and memory cell width. 1): Normal 2): Best and simplest 3): first 4): None of the Given Correct Option: 2 From: Lecture 1 |
| Question # 9 Control bus is only the mechanism. The responsibility of sending the appropriate signals on the control bus to the memory is of the 1): Data Bus 2): processor 3): Address Bus 4): None of the Given Correct Option: 2 From: Lecture 1 Question # 10 In "total: dw 0" Opcode total is a 1): Literal |
| 2): Variable 3): Label 4): Starting point Correct Option: 3 From: Lecture 10 |
| Question # 11 0 1 1 0 0 0 0 C is a example of 1) : Shl 2) : sar 3) : Shr 4) : Sal Correct Option : 3 From : Lecture 10 |
| Question # 12 C 1 1 0 1 0 0 0 0 is a example of(sar can also be fix here as it is the other name of shl) |

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| 1): ShI 2): sar 3): Shr 4): Sal Correct Option: 1 From: Lecture 10 |
|--|
| Question # 13 ADC has operands. 1): two 2): three 3): Five 4): Zero Correct Option: 2 From: Lecture 10 |
| Question # 14 The basic purpose of a computer is to perform operations, and operations need 1): order 2): nothing 3): operands 4): bit Correct Option: 3 From: Lecture 2 |
| Question # 15 Registers are like a scratch pad ram inside the processor and their operation is very much like normal 1): Number 2): opreations 3): memory cells 4): None of the Given Correct Option: 3 From: Lecture 2 Question # 16 |
| There is a central register in every processor called the and The word size of a processor is defined by the width of its |

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| does not hold data but holds the address of data | | |
|--|--|--|
| 1) : Pointer, Segment, or Base Register | | |
| 2) : Pointer, Index, or Base Register | | |
| 3): General Registers | | |
| 4): Instruction Pointer | | |
| Correct Option : 2 From : Lecture 2 | | |
| | | |
| Question # 18 | | |
| "The program counter holds the address of the next instruction to be | | |
| <u>"</u> | | |
| 1) : executed. | | |
| 2) : called | | |
| 3) : deleted | | |
| 4) : copy | | |
| Correct Option: 1 From: Lecture 2 | | |
| Question # 19 | | |
| There are types of "instruction groups" | | |
| 1):4 | | |
| 2):5 | | |
| 3):3 | | |
| 4):2 | | |
| Correct Option: 1 From: Lecture 2 | | |
| Question # 20 | | |
| These instructions are used to move data from one place to another. | | |
| 1): TRUE | | |
| 2): FALSE | | |
| 3): | | |
| 4): Correct Option: 1 From: Lecture 3 | | |
| Correct Option: 1 From: Lecture 2 | | |
| Question # 21 | | |
| "mov" instruction is related to the Group. | | |
| 1) : Arithmetic and Logic Instructions | | |
| 2) : Data Movement Instructions | | |
| 3) : Program Control Instructions | | |
| 4) : Special Instructions | | |
| Correct Option : 2 From : Lecture 2 | | |
| Contest Option : 2 i form : Locatio 2 | | |
| Question # 22 | | |
| allow changing specific processor behaviors and are used | | |
| to play with it. | | |

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| 1) : Special Instructions |
|--|
| 2) : Data Movement Instructions |
| 3) : Program Control Instructions |
| 4): Arithmetic and Logic Instructions |
| Correct Option: 1 From: Lecture 2 |
| Question # 23 |
| 8088 is a 16bit processor with its accumulator and all registers of |
| 1) : 32 bits |
| 2) : 6 bits |
| 3): 16 bits |
| 4): 64 bits |
| Correct Option : 3 From : Lecture 2 |
| Question # 24 |
| The of a processor means the organization and |
| functionalities of the registers it contains and the instructions that |
| are valid on the processor. |
| 1) : Manufactures |
| 2) : architecture |
| 3): Deal |
| 4) : None of the Given |
| Correct Option : 2 From : Lecture 2 |
| Question # 25 |
| Intel IAPX88 Architecture is |
| 1) : More then 25 old |
| 2): New |
| 3) : Not Good |
| 4): None of the Given |
| Correct Option: 1 From: Lecture 2 |
| Question # 26 |
| The iAPX88 architecture consists ofregisters. |
| 1):13 |
| 2):12 |
| 3):9 |
| 4):14 |
| Correct Option : 4 From : Lecture 3 |
| Question # 27 |
| General Registers are |
| 1): AX, BX, CX, and DX |
| 2): XA, BX, CX, and DX |

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| 3): SS,SI and DI 4): 3 Correct Option: 1 From: Lecture 3 | | |
|---|--|--|
| Question # 28 AX means we are referring to the extended 16bit "A" register. Its upper and lower byte are separately accessible as 1): AH and AL 2): A Lower and A Upper 3): AL, AU 4): AX Correct Option: 1 From: Lecture 3 | | |
| Question # 29 AX is General purpose Register where A stands for 1): Acadmic 2): Ado 3): Architecture 4): Accumulator Correct Option: 4 From: Lecture 3 | | |
| Question # 30 The B of BX stands forbecause of its role in memory addressing. 1): Busy 2): Base 3): Better 4): None of the Given Correct Option: 2 From: Lecture 3 | | |
| Question # 31 The D of DX stands for Destination as it acts as the destination in | | |
| 1): I/O operations 2): operations 3): memory cells 4): Memory I/O operations Correct Option: 1 From: Lecture 3 | | |
| Question # 32 The C of CX stands for Counter as there are certain instructions that work with an automatic count in the | | |

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| 1): DI register 2): BX register 3): CX register 4): DX register Correct Option: 3 From: Lecture 3 | | |
|---|--|--|
| Question # 33are the index registers of the Intel architecture which hold address of data and used in memory access. 1): SI and SS 2): PI and DI 3): SI and IP 4): SI and DI Correct Option: 4 From: Lecture 3 | | |
| Question # 34 In Intel IAPX88 architecture is the special register containing the address of the next instruction to be executed. 1): AX 2): PI 3): IP 4): SI Correct Option: 3 From: Lecture 3 | | |
| Question # 35 SP is a memory pointer and is used indirectly by a set of | | |
| 1): instructions 2): Pointers 3): Indexes 4): Variables Correct Option: 1 From: Lecture 3 | | |
| Question # 36is also a memory pointer containing the address in a | | |
| special area of memory called the stack. 1): SP 2): BP | | |
| 3) : PB 4) : AC | | |
| Correct Option: 1 From: Lecture 3 Ouestion # 37 | | |

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| is bit wise significant and accordingly each bit is named | | | |
|--|--|--|--|
| separately. | | | |
| 1): AX | | | |
| 2) : FS | | | |
| 3): IP | | | |
| 4) : Flags Register | | | |
| Correct Option: 4 From: Lecture 3 | | | |
| · | | | |
| Question # 38 | | | |
| When two 16bit numbers are added the answer can be 17 bits long, this | | | |
| extra bit that won't fit in the target register is placed in the | | | |
| where it can be used and tested | | | |
| 1) : carry flag | | | |
| 2) : Parity Flag | | | |
| 3) : Auxiliary Carry | | | |
| 4) : Zero Flag | | | |
| Correct Option: 1 From: Lecture 3 | | | |
| Question # 39 | | | |
| Program is an ordered set of instructions for the processor. | | | |
| 1): TRUE | | | |
| 2) : FALSE | | | |
| 3): | | | |
| 4): | | | |
| Correct Option: 1 From: Lecture 3 | | | |
| Question # 40 | | | |
| For Intel Architecture "operation destination, source" is way of writing things. | | | |
| 1): TRUE | | | |
| 2): FALSE | | | |
| 3): | | | |
| 4): | | | |
| Correct Option: 1 From: Lecture 3 | | | |
| | | | |
| Question # 41 | | | |
| Operation code " add ax, bx " | | | |
| 1) : Add the bx to ax and change the bx | | | |
| 2): Add the ax to bx and change the ax | | | |
| 3) : Add the bx to ax and change the ax | | | |
| 4): Add the bx to ax and change nothing | | | |
| Correct Option: 3 From: Lecture 3 | | | |
| Question # 42 | | | |

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| The maximum memory iAPX88 can a | access is |
|--|---|
| 1): 1MB | |
| 2): 2MB | tp://www.vustudents.net |
| ·/· · ···- | tp.//www.vustudents.net |
| 4) : 128MB | |
| Correct Option : 1 From : Lecture 4 | |
| Question # 43 | |
| The maximum memory iAPX88 can a | access is 1MB which can be accessed with |
| 1): 18 bits | |
| 2): 20 bits | |
| 3): 16 bits | |
| 4): 2 bits | |
| Correct Option : 2 From : Lecture 4 | |
| Question # 44 | |
| address of 1DED0 w | where the opcode B80500 is placed. |
| 1) : physical memory | |
| 2): memory | |
| 3) : efective | |
| 4): None of the Given | |
| Correct Option : 1 From : Lecture 4 | |
| Question # 45 | |
| 16 bit of Segment and Offset Addres | ses can be converted to 20bit Address i.e |
| Segment Address with lower four bits | s zero + Offset Address with |
| four bits zero = 20bit Physical Addres | |
| 1): Middle | |
| 2): lower | |
| 3) : Top | |
| 4): upper | |
| Correct Option : 4 From : Lecture 4 | |
| Question # 46 | |
| When adding two 20bit Addresses a | carry if generated is dropped |
| without being stored anywhere and tl | |
| address | |
| 1) : wraparound | |
| 2) : mode | |
| 3) : ping | |
| 4) : error | |

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| Correct Option: 1 From: Lecture 4 |
|--|
| Question # 47 segments can only be defined a 16byte boundaries called boundaries. 1) : segment 2) : paragraph 3) : Cell 4) : RAM Correct Option : 2 From : Lecture 4 |
| Question # 48 in a Program CS, DS, SS, and ES all had the same value in them. This is called 1): equel memory 2): overlapping segments 3): segments hidding 4): overlapping SI Correct Option: 2 From: Lecture 4 |
| Question # 49 "db num1" size of the memory is 1): 1byte 2): 4bit 3): 16bit 4): 2byte Correct Option: 1 From: Lecture 5 Question # 50 " 1[org 0x0100] 2mov ax, [num1]; load first number in ax 3mov bx, [num2]; load second number in bx 4int 0x21 6 7num1: dw 5 8num2: dw 10 |
| Comments for the 4 are : 1) : No comments Will be 2) : ; accumulate sum in add |

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| 3):; accumulate sum in ax 4):; accumulate sum in Bx Correct Option: 3 From: Lecture 5 | |
|--|--|
| Question # 51 In " mov ax, bx " is Addressing Modes. 1) : Immediate 2) : Indirect 3) : Direct 4) : Register Correct Option : 4 From : Lecture 5 | |
| Question # 52 In "mov ax, [bx]" is Addressing Modes 1): Based Register Indirect 2): Indirect 3): Base Indirect 4): Immediate Correct Option: 1 From: Lecture 5 | |
| Question # 53 In "mov ax, 5" is Addressing Modes 1): Immediate 2): Indirect 3): Indirect 4): Register Correct Option: 2 From: Lecture 6 | |
| Question # 54 In " mov ax, [num1+bx] " is ADDRESSING 1) : OFFSET+ Indirect 2) : Register + Direct 3) : Indirect + Reference 4) : BASEd REGISTER + OFFSET Correct Option : 4 From : Lecture 7 | |
| Question # 55 "base + offset addressing " gives This number which came as the result of addition is called the 1): Address 2): mode | |

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| 3) : effective address |
|---|
| 4) : Physical Address |
| Correct Option : 3 From : Lecture 7 |
| Question # 56 |
| "mov ax, [cs:bx]" associates for this one instruction |
| 1) : CS with BX |
| 2): BX with CS |
| 3) : BX with AX |
| 4) : None of the Given |
| Correct Option : 2 From : Lecture 7 |
| Question # 57 |
| For example |
| BX=0100 |
| DS=FFF0 |
| And Opcode are; |
| move [bx+0x0100], Ax |
| now what is the effective memory address; |
| 1):0020 |
| 2):0200 |
| 3):0300 |
| 4): 0x02 |
| Correct Option : 2 From : Lecture 7 |
| Question # 58 |
| For example |
| BX=0100 |
| DS=FFF0 |
| And Opcode are; |
| move [bx+0x0100], Ax |
| now what is the physical memory address; |
| 1):0020 |
| 2) : 0x0100 |
| 3): 0x10100 |
| 4): 0x100100 |
| Correct Option : 2 From : Lecture 7 |
| Question # 59 |
| In "mov [1234], al "is Addressing Modes. |
| 1) : Immediate |
| 2): Indirect |

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| 3): Direct4): RegisterCorrect Option: 3 From: Lecture 8 | |
|--|----------------|
| Question # 60 In "mov [SI], AX" is Add 1): Basef Register Indirect 2): Indirect 3): Indexed Register Indirect 4): Immediate Correct Option: 3 From: Lecture 8 | ressing Modes. |
| Question # 61 In "mov ax, [bx - Si] " is AD 1): Basef Register Indirect 2): Indirect 3): Direct 4): illegal Correct Option: 4 From: Lecture 8 | DRESSING |
| Question # 62 In "mov ax, [BL] " there is error i.e 1): Address must be 16bit 2): Address must be 8bit 3): Address must be 4bit 4): 8 bit to 16 bit move illegal Correct Option: 4 From: Lecture 8 | |
| Question # 63 In "mov ax, [SI+DI] " there is error i.e 1): Two indexes can't use as Memory Ad 2): index can't use as Memory Address 3): I don't Know 4): None of the Given Correct Option: 1 From: Lecture 8 | |
| Question # 64 In JNE and JNZ there is difference for onl 1): Programmer or Logic 2): Assembler 3): Debugger | у |

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| 4) : IAPX88 |
|--|
| Correct Option: 1 From: Lecture 9 |
| Question # 65 |
| JMP is Instruction that on executing take jump regardless of the state |
| of all flags is called |
| 1): Jump |
| 2) : Conditional jump |
| 3) : Unconditional jump |
| 4): Stay |
| Correct Option : 3 From : Lecture 9 |
| Question # 66 |
| When result of the source subtraction from the destination is zero, |
| zero flag is set i.e. ZF=1 |
| its mean that; |
| 1) : DEST = SRC |
| 2) : DEST != SRC |
| 3): DEST < SRC |
| 4): DEST > SRC |
| Correct Option: 1 From: Lecture 9 |
| Question # 67 |
| When an unsigned source is subtracted from an unsigned destination and |
| the destination is smaller, borrow is needed which sets the |
| 1) : carry flag i.e CF = 0 |
| 2) : carry flag i.e CF = 1 |
| 3) : Carry Flag + ZF=1 |
| 4) : None of the Given |
| Correct Option : 2 From : Lecture 9 |
| Question # 68 |
| In the case of unassigned source and destination when subtracting and |
| in the result ZF =1 OR CR=1 then |
| 1) : DEST = SRC |
| 2) : DEST != SRC |
| 3): UDEST? USRC |
| 4): DEST > SRC |
| Correct Option: 3 From: Lecture 9 |
| Question # 69 |
| In the case of unassigned source and destination when subtracting and |
| in the result ZF =0 AND CR=0 then |

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| 1): DEST = SRC |
|--|
| 2) : DEST != SRC |
| 3) : UDEST < USRC |
| 4): UDEST > USRC |
| Correct Option : 4 From : Lecture 9 |
| Question # 70 |
| In the case of unassigned source and destination when subtracting and |
| in the result CR=0 then |
| 1) : DEST = SRC |
| 2) : DEST != SRC |
| 3) : UDEST < USRC |
| 4): UDEST ? USRC |
| Correct Option : 4 From : Lecture 9 |
| Question # 71 |
| This jump is taken if the last arithmetic operation produced a |
| zero in its destination. After a CMP it is taken if both operands were |
| equal. |
| 1): Jump if zero(JZ)/Jump if equal(JE) |
| 2) : Jump if equal(JE) |
| 3) : Jump if zero(JZ) |
| 4): No Jump fot This |
| Correct Option : 1 From : Lecture 9 |
| Question # 72 |
| This jump is taken after a CMP if the unsigned source is |
| smaller than or equal to the unsigned destination. |
| 1) : JBE(Jump if not below or equal) |
| 2) : JNA(Jump if not above)/JBE(Jump if not below or equal) |
| 3) : JNA(Jump if not above) |
| 4): No Jump fot This |
| Correct Option : 2 From : Lecture 9 |
| Question # 73 |
| Numbers of any size can be added using a proper combination of |
| 1) : ADD and ADC |
| 2) : ABD and ADC |
| 3) : ADC and ADC |
| 4) : None of the Given |
| Correct Option : 1 From : Lecture 11 |
| Question # 74 |
| Like addition with carry there is an instruction to subtract with |
| borrows called . |

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| 1): SwB 2): SBB 3): SBC 4): SBBC Correct Option: 2 From: Lecture 11 |
|---|
| Question # 75 if "and ax, bx" instruction is given, There are operations as a result 1): 16 AND 2): 17 AND 3): 32 AND 4): 8 AND Correct Option: 1 From: Lecture 12 |
| Question # 76 |
| can be used to check whether particular bits of a number are set or not. 1): AND 2): OR 3): XOR 4): NOT Correct Option: 1 From: Lecture 12 Question # 77can also be used as a masking operation to invert selective bits. 1): AND 2): OR 3): XOR 4): NOT Correct Option: 3 From: Lecture 12 |
| Question # 78 Masking Operations are Selective Bit |
| Question # 79 The instruction allows temporary diversion and therefore |

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| reusability of code. | |
|--|--------|
| 1) : CALL | |
| 2) : RET | |
| 3) : AND | |
| 4) : XOR | |
| Correct Option : 1 From : Lecture 13 | |
| | |
| Question # 80 | |
| CALL takes a label as and execution starts from tha | label, |
| 1) : argument | |
| 2): Lable | |
| 3) : TXt | |
| 4): Register | |
| Correct Option: 1 From: Lecture 13 | |
| | |
| Question # 81 | |
| When theinstruction is encountered and it takes execution | วท |
| back to the instruction following the CALL. | |
| 1) : CALL | |
| 2) : RET | |
| 3) : AND | |
| 4) : XOR | |
| Correct Option: 2 From: Lecture 13 | |
| Question # 82 | |
| Both the instructions are commonly use | d as a |
| pair, however technically they are independent in their operation. | |
| 1) : RET and ADC | |
| 2) : Cal and SSb | |
| 3) : CALL and RET | |
| 4) : ADC and SSB | |
| Correct Option : 3 From : Lecture 13 | |
| Overting # 00 | |
| Question #83 | hanaa |
| The CALL mechanism breaks the thread of execution and does not c | lange |
| registers, except | |
| 1) : SI 2) : IP | |
| 3) : DI | |
| 4) : SP | |
| Correct Option: 2 From: Lecture 13 | |

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| Question # 84 |
|--|
| Stack is a that behaves in a first in last out manner. |
| 1) : Program |
| 2) : data structure |
| 3) : Heap |
| 4) : None of the Given |
| Correct Option : 2 From : Lecture 14 |
| Question # 85 |
| If is not available, stack clearing by the callee is a |
| complicated process. |
| 1) : CALL |
| 2) : SBB |
| 3) : RET n |
| 4) : None of the Given |
| Correct Option: 3 From: Lecture 14 |
| Question # 86 |
| When the stack will eventually become full, SP will reach 0, and |
| thereafter wraparound producing unexpected results. This is called |
| stack |
| 1) : Overflow |
| 2): Leakage |
| 3): Error |
| 4) : Pointer |
| Correct Option : 1 From : Lecture 14 |
| Question # 87 |
| The pop operation makes a copy from the top of the stack into |
| its |
| 1): Register |
| 2) : operand |
| 3) : RET n |
| 4) : Pointer |
| Correct Option : 2 From : Lecture 14 |
| Question # 88 |
| decrements SP (the stack pointer) by two and then |
| transfers a word from the source operand to the top of stack |
| 1): PUSH |
| 2) · POP |

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| 3) : CALL 4) : RET | http://www.vustudents.net |
|--|-----------------------------|
| Correct Option: 1 From: Lecture 14 | |
| Question # 89 | |
| POP transfers the word at the current top | of stack (pointed to by SP) |
| to the destination operand and then | SP by two to point to |
| the new top of stack. | |
| 1) : increments | |
| 2) : dcrements | |
| 3):++ | |
| 4): | |
| Correct Option : 1 From : Lecture 14 | |
| Question # 90 | |
| The trick is to use theand | |
| callers' value on the stack and recover it f | from there on return. |
| 1) : POP, ADC | |
| 2) : CALL, RET | |
| 3) : CALL, RET n | |
| 4): PUSH, POP | |
| Correct Option: 4 From: Lecture 14 | |
| Question # 91 | the immediate idea that |
| To access the arguments from the stack, strikes is to them off the stack | |
| 1) : PUSH | or. |
| 2) : POP | |
| 3) : CALL | |
| 4) : Rrgister | |
| Correct Option : 2 From : Lecture 15 | |
| Question # 92 | |
| push bp | |
| we are | |
| 1) : sending bp copy to stack | |
| 2) : making bp copy from stack | |
| 3) : pushing bp on the stack | |
| 4) : doing nothing | |
| Correct Option : 3 From : Lecture 15 | |
| Question # 93 | t sale a |
| Local Variables means variables that are | used within the |

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| 1): Subroutine 2): Program 3): CALL 4): Label Correct Option: 1 From: Lecture 15 |
|---|
| Question # 94 Standard ASCII has 128 characters with assigned numbers from 1): 1to 129 2): 0 to 127 3): 0 to 128 4): None of the Given Correct Option: 2 From: Lecture 16 |
| Question # 95 When is sent to the VGA card, it will turn pixels on and off in such a way that a visual representation of 'A' appears on the screen. 1): 0x60 2): 0x90 3): 0x30 4): 0x40 Correct Option: 4 From: Lecture 16 |
| Question # 96 Which bit is refer to the Blinking of foreground character 1): 6 2): 7 3): 5 4): 3 |
| 1. Assembly language is not a low level language.a. Trueb. False |
| 2. In case of COM File first command parameter is stored at offset of program segment prefix. a. 0x80 (Not Confirm) b. 0x82 |

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| c. 0x84 d. 0x86 |
|--|
| 3. Address always goes from a. Processor to meory b. Memory to processor c. Memory to memory d. None of the above |
| 4. The sourse register in OUT is a. AL or AX b. BL or BX c. CL or CX d. DL or DX |
| 5. By default CS is associated with a. SS b. BP c. CX d. IP |
| 6. Which of the following pins of parallel port are grounded a. 10-18 b. 18-25 c. 25-32 d. 32-39 |
| 7. In the instruction mov word [es:160], 0x1230, 30 represents the character a. A b. B c. 0 d. 1 |
| 8. On executing 0x21 0x3D, if file cant be opened then a. CF will contain 1 b. CF will contain 0 c. ZF will contain 1 d. ZF will contain 0 |

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9. Which of the following IRQ is cascading interrupt

a. IRQ 0

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| b. IRQ 1 c. IRQ 2 d. IRQ 3 |
|---|
| 10. The execution of instruction mov word [es:160], 0x1230, will print a character on the screen at a. First column of second row b. Second column of first row c. Second column of second row d. First column of third row |
| One screen location corresponds to a |
| Byte |
| Word |
| Double byte |
| Double word |
| After the execution of "PUSH AX" statement |
| AX register will reside on the stack |
| A copy of AX will go on the stack |
| The value of AX disappear after moving on stack |
| Stack will send an acceptance message |
| physical address of the stack is obtained by |
| SS:SP combination |

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SS:SI combination

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| SS:SP combination |
|---|
| ES:BP combination |
| ES:SP combination |
| If the address of memory location Num1 is 0117 and its content is 0005 then after execution of the instruction "mov bx, Num1" bx will contain 0005 0117 Num1 1701 |
| In STOS instruction, the implied source will always be in |
| AL or AX registers |
| DL or DX registers |
| BL or BX registers |
| CL or CX registers |
| The shift logical right operation inserts |
| A zero at right |
| A zero at left |
| A one at right |
| A one at right |

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| REP will always |
|---|
| Increment CX by 1 |
| Increment CX by 2 |
| Decrement CX by 1 |
| Decrement CX by 2 |
| |
| When an item is pushed on the decrementing stack, the top of the stack is |
| First decremented and then element copied on to the stack |
| First incremented and then element copied on to the stack |
| Decremented after the element copied on to the stack |
| Incremented after the element copied on to the stack |
| assembly the CX register is used normally as aregister. |
| source |
| counter |
| index |
| pointer |
| Which is the unidirectional bus ? |
| (I) Control Bus |
| (II) Data Bus |
| (III) Address Bus |
| I only |
| II only |
| |

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III only

I and II only

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| The basic function of SCAS instruction is to |
|---|
| Compare |
| Scan |
| Sort |
| Move data |
| register holds the address of next instruction is to be executed Base pointer Program counter |
| JC and JNC test the flag. carry In string manipulation whenever an instruction needs a memory source, which of the following will hold the pointer to it? |
| ES: DI |
| which bit sets the character "blinking" on the screen? |
| 7 |
| If we want to divide a signed number by 2, this operation can better be accomplished by SAR |
| After the execution of STOSWB, the CX wil be |
| Decremented by 1 |
| Each screen location corresponds to a word, the lower byte of this word contains |
| The character code In a video memory, each screen location corresponds to |
| Two bytes |